GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

DIGITAL ELECTRONICS

Course Code: GR15A2043 L:3 T:1 P:0 C:4
II Year II Semester

Prerequisites
- Basics of number systems and Electronic devices and circuitry
- Basics of De-Morgan's Laws

Course Objectives
- Create minimal realizations of single and multiple output Boolean functions.
- Derive the digital circuits using flip-flops, counters and registers
- Derive state diagrams and state transition tables for synchronous systems.

Course Outcomes
- Ability to apply knowledge of digital theory enables the process of logical design.
- Ability to analyze and design a registers, counters with the help of flip-flops.
- Demonstrate knowledge of hazards and race conditions generated within asynchronous circuits.

Unit-I
Number systems and Boolean algebra: Digital systems, Number - Base Conversions, Octal and Hexa-decimal Numbers, Complements, Signed Binary Numbers, Binary Codes, Binary Storage and Registers, Binary Logic, Axiomatic Definition of Boolean Algebra, Basic Theorems and Properties of Boolean Algebra, Boolean Functions, Canonical and standard Forms, Other Logic Operations

Unit-II
Logic Gates: Digital Logic Gates, Integrated Circuits, Gate-level Minimization, The Map Method, Four- Variable Map, Five-Variable Map, Product-of-Sums Simplification, Don't-care Conditions, NAND and NOR Implementation, Exclusive-OR Function.

Unit-III
Combinational logic: Introduction to Combinational circuits, Analysis Procedure, Design Procedure, Code-conversion, Binary Adder - Subtractor,

Carry Propagation, Half Subtractor, Full Subtractor, Binary Subtractor, Decimal Adder, BCD adder, Binary Multiplier, Magnitude Comparator, Decoders, Encoders, and Multiplexers with design examples.

Unit-IV

Sequential Logic: Flip-Flops, Triggering of Flip Flops, Analysis of Clocked Sequential Circuits, State Reduction and Assignment, Flip-Flop Excitation Tables, Design Procedure, Fundamentals of Asynchronous Sequential Logic: Introduction, Analysis procedure, Circuits with Latches, Design Procedure, Hazards.

Unit-V

Registers and Counters: Registers with parallel load, Shift registers; Serial Transfer, Serial Addition, Universal Shift Register, Ripple Counters; Binary Ripple Counter, BCD Ripple Counter, Synchronous Counters; Binary Counter, Up-Down Counter, BCD Counter, Binary Counter with Parallel Load, Counter with Unused States, Ring Counter, Johnson Counter.

Teaching Methodologies

1. Power Point presentations
2. Tutorial Sheets
3. Assignments
4. Lab experiments with Xlinix software

Text Books

1. M. Morris Mano and Michael D. Ciletti, Digital Design, Fourth Education, Pearson 5th ed2013.
2. Charles H. Roth JR. Larry L. Kinney, Fundamentals of Logic Design, Cengaue learning 6th edition,2013.

Reference Books

1. ZviKohavi,SwitcshingandFiniteAutomataTheory,2ndEdition,TMH
2. FrederickJ.Hill and GeraldR Peterson, Introductionto Switchingtheory and logicdesign, 3rdEdition, JohnWileyandsons,1981.
3. Switching Theory and Logic Design by A. Anand Kumar, 2nd Edition, PHI Publishers.