GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

COMPUTER ORGANIZATION

Course Code: GR15A2076 L:3 T:1 P:0 C:4
II Year II Semester

Prerequisites: Knowledge of Digital Logic Design.

Course Objectives
- Comprehend operational concepts and understand register organization in a basic computer system.
- Analyze the basic computer organization and understand the concepts of Micro programmed control.
- Understand the design of Central processing unit organization and various arithmetic operations with algorithms.
- To study the different ways of communicating with I/O devices and standard I/O interfaces.
- To study the hierarchical memory system including cache memory and virtual memory.

Course Outcomes
- Students should be able to demonstrate knowledge of register organization of a basic computer system.
- To incorporate In-depth understanding of control unit organization and micro programmed control.
- Students should be able to perform arithmetic operations and understand the performance of central processing unit of a basic computer system.
- To analyze and emphasize various communication media in the basic computer system.
- Develop an ability to analyze and design various memory structures.

Unit-I
Basic Structure of Computers: Computer Types, Functional unit, Data Representation, Fixed Point Representation, Floating – Point Representation, Error Detection codes.

Register Transfer Language and Micro operations: Register Transfer language, Register Transfer, Bus and memory transfers, Arithmetic Micro operations, Logic micro operations, Shift micro operations, Arithmetic logic shift unit.

Unit-II

Basic Computer Organization and Design: Instruction codes, Computer Registers, Computer instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt, Complete Computer Description.

Micro Programmed Control: Control memory, Address sequencing, micro program example, design of control unit, Micro program Sequencer, Hard wired control Vs Micro programmed control.

Unit-III

Central Processing Unit Organization: General Register Organization, STACK organization, Instruction formats, Addressing modes, DATA Transfer and manipulation, Program control, Reduced Instruction Set Computer.

Computer Arithmetic: Addition and subtraction, multiplication Algorithms, Floating – point Arithmetic operations, BCD Adder.

Unit-IV

Input-Output Organization: Peripheral Devices, Input-Output Interface, Asynchronous data transfer Modes of Transfer, Priority Interrupt, Direct memory Access, Input –Output Processor (IOP).

Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, Dependencies, Vector Processing.

Unit-V

Memory Organisation: Memory Hierarchy, Main memory- RAM and ROM chips, Memory Address map, Auxiliary memory – Magnetic Disks, Magnetic Tapes, Associative Memory – Hardware Organization, Match Logic, Cache Memory – Associative mapping, Direct mapping, Set associative mapping, Writing into cache and cache initialization, Cache Coherence, Virtual memory – Address Space and Memory Space, Address mapping using pages, Associative Memory page table, Page Replacement.
Multi Processors: Characteristics or Multiprocessors, Interconnection Structures, Cache Coherence, Shared Memory Multiprocessors.

Teaching Methodologies

1. Power Point Presentations
2. Tutorial Sheets
3. Assignments

Text Books

1. Computer Systems Architecture – M.Moris Mano, IIIrd Edition, Pearson/PHI
2. Computer Organization – Carl Hamacher, Zvonks Vranesic, SafeaZaky, Vth Edition, McGraw Hill.

Reference Books

1. Computer Organization and Architecture – William Stallings Sixth Edition, Pearson/PHI
2. Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition PHI/Pearson
3. Fundamentals or Computer Organization and Design, - Sivaraama Dandamudi Springer Int. Edition.
4. Computer Architecture a quantitative approach, John L. Hennessy and David A. Patterson, Fourth Edition Elsevier 5. Computer Architecture: Fundamentals and principles of Computer Design, Joseph D. Dumas II, BS Publications.