GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

DIGITAL ELECTRONICS LAB

Course Code: GR152053 L:0 T:0 P:2 C:2
II Year I Semester

Course Objectives
- To Simulate digital combinational circuits using VHDL
- To Simulate digital sequential circuits using VHDL

Course Outcomes
- Ability to apply knowledge of digital theory enables the process of logical design.
- Ability to simulate digital combinational circuits using VHDL
- Ability to simulate digital sequential circuits using VHDL

LIST OF EXPERIMENTS
1.DESIGN AND SIMULATION OF COMBINATIONAL CIRCUITS USING VHDL

Experiment 1: Realization of Gates
Experiment 2: Half adder, Full adder
Experiment 3: Magnitude comparator
Experiment 4: Decoder
Experiment 5: Multiplexer
Experiment 6: Demultiplexer
Experiment 7: Binary to Grey Code Converter
Experiment 8: Parity Checker

2.DESIGN AND SIMULATION OF SEQUENTIAL CIRCUITS USING VHDL

Experiment 9: D and T Flip-Flops
Experiment 10: Frequency Divider
Experiment 11: Left Shift Register
Experiment 12: Serial to Parallel Shift Register
Experiment 13: Binary Counter
Experiment 14: Asynchronous BCD Up Counter
Experiment 15: Synchronous Down Counter

Note: A minimum of 12 (Twelve) experiments have to be performed and recorded by the candidate to attain eligibility for Practical Examination.

Lab methodologies
- Assignments
- Lab experiments with Xlinix Software