TEQIP II - Sponsored
Faculty Development Programme
on
VLSI Digital Signal Processing
28th to 30th January 2016

Registration Form

Name:

Institution/Organization:

Qualification:

Designation:

Email ID:

Phone Number:

Official Contact Address:

Payment Details:
(DD must be drawn in the favor of **GRIET ECE, Payable at Oriental Bank of Commerce, Hyderabad)**

DD No:

DD Date:

Name of the Bank:

Amount:

Date:

Place: Signature of Applicant

Signature & office seal with date of
Head of the Institution/Organization

Chief Patrons
Prof. P.S. Raju, Director, GRIET
Dr. J. N. Murthy, Principal, GRIET
Dr. K.V.S. Raju, Senior A.O, GRIET

Advisor
Dr.T.C.Sarma, HOD, Department of ECE

Convener
Dr.G.Mamatha, Professor, GRIET

Organizing Committee
Mr. M. Kiran, Associate Professor
Mr. K.Jamal, Associate Professor
Mr.M.O.V.Pavan Kumar, Asst. Professor
Ms. K. Nagaja, Asst. Professor.
Ms. A. UshaSree, Asst. Professor.
Ms. G.L.Sumalata, Asst. Professor.
Ms .R. Naga Pavani, Asst. Professor.
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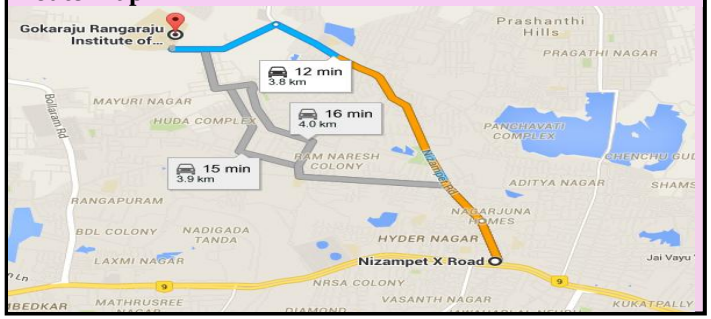
Contact
Send your registration details (soft copy) to vlsisp@griet.in
For further information
Ms. A. UshaSree, 9291657212
Mr. K. Jamal, 9666975786

Route Map



Griet
Gokaraju Rangaraju Institute of Engineering & Technology
1997

Faculty Development Program
on
VLSI Digital Signal Processing
28th to 30th January, 2016

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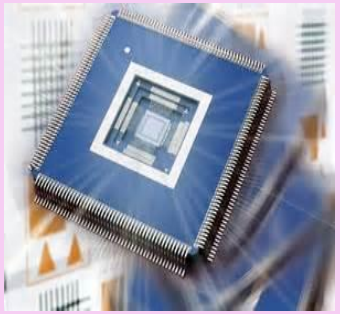
TEQIP II



Organized by
Department of Electronics and Communication Engineering

Gokaraju Rangaraju Institute of Engineering and Technology
(Autonomous)
Bachupally, Hyderabad-90

About the Institution

Gokaraju Rangaraju Institute of Engineering and Technology (GRIET) is a premier institute established in 1997 under the patronage of the Gokaraju Rangaraju Educational Society. The institute is comprised of, among others, the Departments of Electronics and Communication Engineering (ECE), Electrical and Electronics Engineering (EEE), Computer Science and Engineering (CSE), Information Technology (IT), Mechanical Engineering (ME), Civil Engineering (CE), Biomedical Engineering (BME) and Bio-Technology (BT).

Graduate Programs are offered by ECE, EEE, CSE, IT and ME. The Institute also offers MCA and MBA Programs. GRIET is an autonomous institution, affiliated to JNTU, Hyderabad, and is approved by AICTE. The Departments of ECE, EEE, BT, CSE, IT and MCA are accredited by the NBA & NAAC.

About the Department

The Department of Electronics and Communication Engineering was established in the year 1997.

The Department has well-equipped Labs such as Communication Lab, Micro Controller Lab, Digital Signal Processing Lab, Microwave & Optical Communication Lab, e-CAD & VLSI Lab. The Department has highly qualified faculty with vast experience. The Department has a well-balanced workforce having experience in academics and in industry.

Objective of FDP

VLSI Digital Signal Processing assumes importance from the point of view of wide spread use of digital signal processors for number of applications in various fields. This FDP aims to provide a broad coverage of techniques for designing efficient DSP architectures.

Emphasis is on the architectural research, design and optimization of signal processing systems. Faculty members will be able to teach and guide students' projects well both at B.Tech and at M.Tech level in this area. Also this FDP will enable them to take up or carry on research work in this area.

Topics to be covered in FDP

1. **VLSI for Health Monitoring Systems**
2. **VLSI DSP –Logic optimization**
3. **VLSI for Wireless applications**
4. **VLSI Wireless applications –Case studies**
5. **Graphical representation of DSP Algorithms**
6. **High level transformations of SFG and DFG**
7. **Retiming a DFG, examples from DSP**
8. **CORDIC algorithm, parallel CORDIC processing, applications from FFT, DCT, Communications**
9. **Parallel realization of DSP algorithms**
10. **Bit serial, digit serial and word serial architectures**
11. **Concept of folding , Area and power minimization**
12. **Bit level architectures, Examples, Homer's rule.**
13. **Bit serial multipliers & design of FIR and IIR filters, examples.**

Resource Persons

1. Dr. Mrityunjoy Chakraborty

Professor, Department of E & ECE

IIT Kharagpur

2. Dr. Amit Acharya

Assistant Professor, Department of Electrical Engineering

IIT Hyderabad

3. Dr. Rahul Shrestha

Assistant Professor, CVEST

IIIT Hyderabad

Registration

Participants should confirm their interest on or before 18-01-2016 by email.

Work Shop Dates: **28th to 30th January 2016**

Registration Fee: Rs. 600.

Includes: Tea, Snacks and Lunch

How to Apply

The applicants should send their registration information through email and are required to submit hardcopy of registration form along with DD in favor of **GRIET ECE, Payable at Oriental Bank of Commerce, Hyderabad.**

OR

For Online/NEFT Transfer
Acc No: 10812041022487
IFSC Code: ORBC0101882
Oriental Bank of Commerce
Bachupally Branch, Hyderabad.

Department of Electronics and Communication Engineering
Email: vlsisp@griet.in
Website: www.griet.ac.in