ACADEMIC REGULATIONS

PROGRAM STRUCTURE

and

DETAILED SYLLABUS

Master of Technology

(VLSI)

(Two Year Regular Programme)

K(Applicable for Batches admitted from 2018

GokarajuRangaraju Institute of Engineering and Technology

(Autonomous)

Bachupally, Kukatpally, Hyderabad- 500 090
# VLSI

## I YEAR - I SEMESTER

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## I YEAR - II SEMESTER

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### Audit course 1 & 2

1. English for Research Paper Writing (GR18D5207)
2. Disaster Management (GR18D5208)
3. Sanskrit for Technical Knowledge (GR18D5209)
4. Value Education (GR18D5210)
5. Indian Constitution (GR18D5211)
6. Pedagogy Studies (GR18D5212)
7. Stress Management by Yoga (GR18D5213)
8. Personality Development through Life Enlightenment Skills. (GR18D5214)
Course Code: GR18D5076

L/T/P/C: 3/0/0/3

Course objectives

- Learn digital design of Sequential Machines.
- Design drawing state graphs.
- Design realization and implementation of SM Charts.
- Design Fault modeling and test pattern generation of Combinational circuits.
- Learn fault diagnosis in sequential circuits and understand machine design, identification of fault detection experiment.

Course outcomes

- Create understanding of the design techniques of sequential Machines.
- Create understanding of the fundamental concepts of PLD's, design of FPGA's.
- Learn implementation of SM charts in combinational and sequential circuits.
- Develop skills in modeling fault free combinational circuits.
- Develop skills in modeling Sequential circuits in terms of reliability, availability and safety.

Unit I: DIGITAL SYSTEM DESIGN AUTOMATION AND RTL DESIGN WITH VERILOG


Unit II: VERILOG LANGUAGE CONCEPTS

Characterizing Hardware Languages, Module Basics, Verilog Simulation Model, Compiler Directives, System Tasks and Functions

Unit III: COMBINATIONAL CIRCUIT DESCRIPTION

Module Wires, Gate Level Logic, Hierarchical Structures, Describing Expressions with Assign statements, Behavioral Combinational Descriptions, Combinational Synthesis.

Unit IV: SEQUENTIAL CIRCUIT DESCRIPTION

Sequential models, Basic Memory Components, Functional Registers, State Machine Coding, Sequential Synthesis. Component Test, Verification and Detailed Modeling, Test Bench, Test Bench Techniques, design Verification, Assertion Verification, Text Based Test Benches, Detailed Modeling- Switch Level Modeling, Strength Modeling.
Unit V: RTL DESIGN AND TEST

Sequential Multiplier- Shift-and- Add Multiplication process, sequential multiplier design, Multiplier testing, Von Neumann Computer Model- Processor and memory model, processor model specification, designing the adding CPU, Design of datapath, Control part design, Adding CPU verilog description, tesing adding CPU

Text Books


Reference Books

Course Code: GR18D5077  
L/T/P/C: 3/0/0/3

Course objectives

- To describe over view about evolution of CMOS integrated circuits.
- To provide knowledge about Combinational, Sequential MOS logic circuits.
- To introduce and familiarize with the various logic circuits.
- To prepare them to face the challenges in dynamic logic circuits.
- To create interest in the integrated circuit design and prepare them to face the challenges in VLSI technology.

Course outcomes

- An ability to know about the various Combinational and Sequential MOS logic circuits.
- An in-depth knowledge of applying the concepts on real time applications
- An ability to know the design of dynamic MOS logic circuits.
- Able to know the design of semiconductor memories.
- An ability to understand the basic concepts of Boolean expressions.

Unit I: MOS DESIGN

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

Unit II: COMBINATIONAL MOS LOGIC CIRCUITS

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

Unit III: SEQUENTIAL MOS LOGIC CIRCUITS

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.
Unit IV: DYNAMIC LOGIC CIRCUITS

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

Unit V: SEMICONDUCTOR MEMORIES

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

Text Books


Reference Books

Course Code: GR18D5078 L/T/P/C: 3/0/0/3

Course Objectives

- Learn digital design of Sequential Machines.
- Learn drawing state graphs.
- Learn realization and implementation of SM Charts.
- Learn Fault modeling and test pattern generation of Combinational circuits.
- Learn fault diagnosis in sequential circuits and understand machine design, identification of fault detection experiment.

Course Outcomes

- Create understanding of the design techniques of sequential Machines.
- Create understanding of the fundamental concepts of PLD's, design of FPGA's.
- Develop skills in modelling Sequential circuits in terms of reliability, availability and safety.
- Develop skills in modelling fault detection experiments of sequential circuits.

Develop skills in modelling combinational circuits in terms of reliability, availability and safety

Unit I: MINIMIZATION AND TRANSFORMATION OF SEQUENTIAL MACHINES


Unit II: DIGITAL DESIGN

Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.
Unit III: SM CHARTS

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

Unit IV: FAULT MODELING & TEST PATTERN GENERATION


Unit V: FAULT MODELING & TEST PATTERN GENERATION

Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

Text Books

3. Logic Design Theory – N. N. Biswas, PHI

Reference Books

Course Code: GR18D5079 L/T/P/C: 3/0/0/3

Course Objectives

• To impart to students knowledge of semiconductor physics and integrated passive devices.
• To enable students to analyze the behavior of monolithic diodes with the help of models of integrated diodes.
• To enable students to analyze the behavior of integrated NMOS and PMOS transistors with the help of SPICE models.
• To enable students visualize different VLSI fabrication techniques of different processes.
• To enable students to model hetero junction devices.

Course Outcomes

• The graduate student will be equipped with knowledge of semiconductor physics.
• The graduate student will be able to relate model parameters to structures of integrated passive devices.
• The graduate will be able to analyze static and dynamic behavior of diodes.
• The graduate student will be able to model electrically NMOS and PMOS transistors.
• The graduate student will be able to use SPICE model level 1, 2, 3 and 4 and hence will be able to analyze various integrated circuits.

Unit I: INTRODUCTION TO SEMICONDUCTOR PHYSICS

Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.

Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

Unit II: INTEGRATED DIODES

Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models

Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon modeldynamic model, Parasitic effects – SPICE model –Parameter extraction
Unit III: INTEGRATED MOS TRANSISTOR

NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4.

Unit IV: VLSI FABRICATION TECHNIQUES


Unit V: MODELING OF HETERO JUNCTION DEVICES

Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe.

Text Books


Reference Books

Course Code: GR18D5080
L/T/P/C: 3/0/0/3

Course objectives

- To describe the need of using scripting language programs.
- To use PERL scripting language at the instances required.
- To apply advanced level PERL for software automation.
- To employ the PERL scripting language for file system navigation.
- To illustrate software automation using TCL.

Course outcomes

- The students will be in a position to judge whether scripting language program is needed for a particular rcode.
- Students will be acquainted with the basic level scripting language programming in PERL.
- Students will be skillful to code in PERL for advanced level software automation.
- Students will have the programming skills to automate the software for event-driven programs too.
- Students will be in a position to demonstrate software automation using Java Script, PERL-TK, and in basic level using python scripting language.

Unit I: INTRODUCTION TO SCRIPTS AND SCRIPTING

Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

Unit II: ADVANCED PERL

Finer points of looping, subroutines, using pack and unpack, working with files, navigating the file system, type globs, eval, references, data structures, packages, libraries and modules, objects, objects and modules in action, tied variables, interfacing to the operating systems, security issues.

Unit III: TCL

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.
Unit IV: ADVANCED TCL


Unit V: TK AND JAVASCRIPT


Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

Text Books


Reference Books

Course Code: GR18D5111

Course objectives

- To understand the concept of Programmable Logic Device architectures and technologies.
- Underlying FPGA architectures and technologies in detail.
- To understand the difference between CPLDs and FPGAs.
- To provide knowledge about SRAM Programmable FPGA Device architecture.
- To comprehend knowledge about Anti-Fuse Programmable FPGA Device architecture.

Course outcomes

- To know the concept of programmable architectures.
- Perceiving CPLD and FPGA technologies.
- Study and compare the different architectures of CPLDs and FPGAs.
- An ability to know the SRAM Technology based FPGAs.
- An ability to know the Anti-Fuse Technology based FPGAs

Unit I: INTRODUCTION TO PROGRAMMABLE LOGIC DEVICES


Unit II: FIELD PROGRAMMABLE GATE ARRAYS

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

Unit III: SRAM PROGRAMMABLE FPGAS


Unit IV: ANTI-FUSE PROGRAMMED FPGAS

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.
Unit V: DESIGN APPLICATIONS

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Text Books


Reference Books

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
Course Code: GR18D5082
L/T/P/C: 3/0/0/3

Course objectives
- To introduce the outline architecture of ARM7 microcontroller including basics of pipelines, registers, exception modes.
- To set up and customize a microcontroller development environment.
- To give an overview of system peripherals which cover bus structure, memory map, register programming and muchmore.
- To write programs that interact with other devices.
- To learn the Memory Management of RISC Microcontrollers.

Course outcomes
- An ability to understand the hardware implementation of the ARM7 microcontrollers.
- An ability to integrate peripherals based on I/O functions.
- An ability to learn the concept of pipelines, registers and exception modes.
- An ability to program in ARM and THUMB modes.
- An ability to interpret the functions of Memory Management Unit (MMU).

Unit I: ARM ARCHITECTURE

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

Unit II: ARM PROGRAMMING MODEL – I

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

Unit III: ARM PROGRAMMING MODEL – II

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

Unit IV: ARM PROGRAMMING

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.
Unit V: MEMORY MANAGEMENT

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

Text Books


Reference Books

Course Code: GR18D5083  L/T/P/C: 3/0/0/3

Course objectives

- To enable the student to visualize MOS fabrication technologies and to understand electrical properties of MOS, CMOS and Bi CMOS circuits.
- To train the student to draw integrated circuit layouts following design rules.
- To enable the student design combinational circuit, do verification, power optimization and network testing.
- To enable the student to use power optimization techniques, design validation procedures and testing of sequential circuits.
- To train the student to use different floor planning methods and different low power architectures.

Course outcomes

- Visualize the steps taken for MOS fabrication technologies.
- Analyze electrical behavior of MOS, CMOS and Bi CMOS circuits.
- Draw the layout of integrated circuits following design rules.
- Design combinational circuit.
- Design sequential circuits using different clocking disciplines.

Unit I: REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

Unit II: LAYOUT DESIGN AND TOOLS

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. 
**Logic Gates & Layouts:** Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

Unit III: COMBINATIONAL LOGIC NETWORKS

Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.
Unit IV: SEQUENTIAL SYSTEMS

Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

Unit V: SEQUENTIAL SYSTEMS


Text Books


Reference Books

Course Code: GR18D5084  
L/T/P/C: 0/0/4/2

Course objectives

This lab deals with programming using Verilog for advanced digital design techniques. It offers board coverage of HDL from a practical design perspective. Introduces students to gate, dataflow(RTL) and behavioral modeling.

Note: All the following digital circuits are to be designed and implemented on FPGA using XILINX’s/ Altera’s/ Equivalent CAD tools.

Programming can be done using any HDL compiler, Verification of the Functionality of the module using functional Simulator, Timing Simulator for Critical Path time Calculation, Synthesis of module, Place & Route and implementation of design using FPGA.

**Task 1**
Digital Circuits Description using Verilog/ VHDL

**Task 2**
Verification of the Functionality of designed Circuits using function Simulator.

**Task 3**
Timing Simulation for critical path time calculation.

**Task 4**
Synthesis of Digital Circuits.

**Task 5**
Place and Route techniques for major FPGA vendors such as Xilinx/ Altera/ Actel etc.

**Task 6**
Implementation of Designed Digital Circuits using FPGA and CPLD devices.
Course Code: GR18D5085  
L/T/P/C: 0/0/4/2

Course objectives

- To describe overview about evolution of CMOS integrated circuits.
- To provide knowledge about Combinational, Sequential MOS logic circuits.
- To introduce and familiarize with the various logic circuits.
- To prepare them to face the challenges in dynamic logic circuits.
- To prepare them to design various building blocks in combinational and sequential circuits.

Course outcomes

- An ability to know about the various Combinational and Sequential MOS logic circuits.
- An in-depth knowledge of applying the concepts on real-time applications.
- An ability to understand the basic concepts of Boolean expressions.
- Able to design different Combinational logic blocks.
- Able to analyze and implement various memory elements.

Task 1
For a given specifications plot the characteristics for NMOS and PMOS transistors by varying \( I_D, V_{DS}, \) and \( V_{GS} \).

Task 2
For a given specifications plot VTC Curve for CMOS Inverter and calculate \( V_{IL}, V_{HI}, NM_H, NM_L \).

Task 3
For a given specifications plot VTC Curve for CMOS Inverter with varying \( V_{DD} \).

Task 4
For a given specifications plot VTC Curve for CMOS Inverter with varying Device size.

Task 5
Perform transient of CMOS inverter with no load and with load and determine \( T_{PHL}, T_{PLH} \).

Task 6
Design and Draw layout for CMOS NOR/ NAND gate and perform DRC, LVS, RC Extraction.

Task 7
Design and Draw layout for CMOS XOR gate using Transmission Gates and perform DRC, LVS, RC Extraction.

Task 8
Design and Draw layout for combinational function using CMOS logic and perform DRC, LVS, RC Extraction.

Task 9
Design and Draw layout for D-Flip Flop using CMOS logic and perform DRC, LVS, RC Extraction.

Note: All the following digital circuits are to be designed and implemented using Cadence/Mentor Graphics/Synopsys/ equivalent CAD Tools.
Course Code: GR18D5012  

Course objectives

- To familiarise students with the different aspects of research.
- To provide an idea of good scientific writing and proper presentation skills.
- To provide an understanding of philosophical questions behind scientific research.
- To provide a brief background on the historical legacy of science.
- To provide an insight of nature of Intellectual Property and new developments in IPR.

Course Outcomes: At the end of this course, students will be able to

- Understand research problem formulation.
- Analyze research related information and follow research ethics
- Understand that today’s world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasise the need of information about Intellectual Property Right to be promoted among students in general & engineering.
- Understand the nature of Intellectual Property and IPR in International scenario.

Unit I
Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

Unit II
Effective literature studies approaches, analysis Plagiarism, Research ethics,

Unit III
Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Unit IV

Unit V
Reference Books

2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”
Course Code: GR18D5086  L/T/P/C: 3/0/0/3

Course objectives

- To describe over view about evolution of CMOS integrated circuits.
- To provide knowledge about fabrication process and technology.
- To introduce and familiarize with the various Amplifiers & OP-amps.
- To prepare them to face the challenges in CMOS technology.
- To design the various comparators and characterize.

Course outcomes

- Able to develop an in-depth understanding of the design principles and applications of CMOS analog IC design.
- An ability to know the fabrication steps involved in CMOS technology.
- Familiar with the small signal and large signal models of CMOS transistors.
- An in-depth knowledge of applying the concepts on real time applications.
- Analyze and design of CMOS op Amps and compensation techniques.

UNIT I: MOS DEVICES AND MODELING


UNIT II: ANALOG CMOS SUB-CIRCUITS

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT III: CMOS AMPLIFIERS

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT IV: CMOS OPERATIONAL AMPLIFIERS

UNIT V: COMPARATORS

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS


REFERENCE BOOKS

3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.
Course Code: GR18D5087

L/T/P/C: 3/0/0/3

Course objectives

• To understand the ASICs and CMOS logic.
• To learn the various synthesis and static timing analysis.
• To learn the implementation design for testability.
• To understand concept of routing techniques.
• To understand the latest design techniques as practiced in the Industry for design layout optimization.

Course outcomes

• Apply the appropriate design practices, software tools, and research methods for IC design.
• Design the systems by using synthesis and static timing analysis.
• Design the low power digital systems by applying appropriate partitioning and Floor planning algorithms.
• Design the real time applications using routing techniques.
• Understand the concepts of geometric programming and convex functions.

Unit I: INTRODUCTION TO ASIC’S AND CMOS LOGIC

Types of ASICs - Design flow - CMOS transistors - CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell-Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

ASIC Library Design and Programmable Technologies

Library cell design - Schematic view of Library architecture - Anti fuse - Static RAM - EPROM and EEPROM technology - PREP benchmarks

Unit II: ASIC VERIFICATION


Unit III: SYNTHESIS AND STATIC TIMING ANALYSIS


Unit IV: DESIGN FOR TESTABILITY


Unit V: PHYSICAL DESIGN

Physical design flow, System partition - Partitioning methods - Floor planning - Placement — Global routing - Detailed routing - Circuit extraction – DRC.

Text Books


Reference Books

Course objectives
- To understand the tradeoffs among various design styles given a set of design constraints in physical design automation and to understand performance/area tradeoffs in a chip design process.
- To learn the various statistic modeling methods like Monte Carlo techniques and Pelgroms model etc.
- To learn the implementation issues for digital design automation including optimization techniques.
- To understand concept of design optimization algorithms and their application to physical design automation.
- To understand the latest design techniques as practiced in the Industry for design layout optimization.

Course outcomes
- Apply the appropriate design practices, emerging technologies, state-of-the-art design techniques, software tools, and research methods for IC design.
- Design the systems by using concepts of High level statistical, Gate level statistical analysis methods.
- Design the low power digital systems by applying appropriate partitioning and Floor planning algorithms.
- Design the real time applications using optimization techniques like Genetic Algorithms.
- Understand the concepts of geometric programming and convex functions.

Unit I: STATISTICAL MODELING
Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgroms model, Principle component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

Unit II: STATISTICAL PERFORMANCE, POWER AND YIELD ANALYSIS
Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

Unit III: CONVEX OPTIMIZATION
Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.
Unit IV: GENETIC ALGORITHM


Unit V: GA ROUTING PROCEDURES AND POWER ESTIMATION


Text Books / Reference Books

Course Code: GR18D5089

Course Objectives

- To describe the system design approach with respect to the hardware and software.
- To apply the techniques for reducing the delays in program execution.
- To categorize and compare different processor types for their selection into a System on Chip.
- To compare different memory designs and their purposes.
- To interpret the architectures and applications of various buses.

Course Outcomes

- Students will be able to summarize all the components required for system design.
- Students will be acquired the techniques to minimize the delays for better performance of a system on chip.
- Students will be able to analyze different types of buses for respective applications.
- Students will be skilful to judge a configurable device based on the application requirement for a system on chip.
- Students will have the technique to implement AES algorithm if required.

Unit I: INTRODUCTION TO THE SYSTEM APPROACH


Unit II: PROCESSORS


Unit III: MEMORY DESIGN FOR SOC

Unit IV: INTERCONNECT CUSTOMIZATION AND CONFIGURATION


Unit V: APPLICATION STUDIES / CASE STUDIES

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG Compression.

Text Books


Reference Books

2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
Course Code: GR18D5090  L/T/P/C: 3/0/0/3

Course objectives

- To provide knowledge about VLSI Testing.
- To understand VLSI Technology Trends affecting Testing.
- To get knowledge on Design verification and Test Evaluation.
- To understand the concept of BIST architecture.
- To provide knowledge about Boundary Scan Test.

Course outcomes

- Create understanding of the fundamental concepts of Testing in VLSI design.
- Perceiving Trends affecting Testing.
- An ability to know the high level testability measures and scan methods.
- An ability to know the BIST architecture: Test pattern generation, Circuit under test and Output response analyzer.
- Develop skills in modeling and evaluating Boundary Scan Standards.

Unit I: INTRODUCTION TO TESTING


Unit II: LOGIC AND FAULT SIMULATION


Unit III: TESTABILITY MEASURES

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

Unit IV: BUILT-IN SELF-TEST

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.
Unit V: BOUNDARY SCAN STANDARD

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Text Books


Reference Books

Course Code: GR18D5091  L/T/P/C: 3/0/0/3

Course objectives

• To provide sound foundation of digital signal processing (DSP) architectures for designing efficient VLSI architectures for DSP systems.
• To analyze general purpose digital signal processors.
• To understand pipelining, parallel processing and retiming.
• To illustrate the features of on-chip peripheral devices and its interfacing along with its programming details.
• To analyze DSP architectures.

Course outcomes

• An ability to recognize the fundamentals of fixed and floating point architectures of various DSPs.
• An ability to learn the architecture details and instruction sets of fixed and floating point DSPs.
• An ability to Infer about the control instructions, interrupts, and pipeline operations.
• AnabilitytoanalyzearndlearntoimplementthesignalprocessingalgorithmsinDSPs.
• An ability to learn the DSP programming tools and use them for applications.

Unit I: INTRODUCTION TO DIGITAL SIGNAL PROCESSING

Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

Unit II: COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

Unit III: ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Unit IV: PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.
Unit V: ANALOG DEVICES FAMILY OF DSP DEVICES


Text Books


Reference Books

Course Code: GR18D5092  L/T/P/C: 3/0/0/3

Course Objectives

- To know about the need for low power circuit design.
- To provide strong foundation of fundamentals of low power circuit design.
- To furnish knowledge of various low power design approaches for VLSI System design.
- To analyze different low power design techniques.
- To develop different low voltage low power logic styles using low power techniques.

COURSE OUTCOMES

- Student develops strong knowledge of fundamentals of low power VLSI circuit design.
- Student will be aware of various low power VLSI design approaches.
- Student will be aware of various low power logic styles.
- Student will be able to analyze all the low power design techniques.
- Student will develop the capability of designing low power data path subsystems such as adders and multipliers.

Unit I: FUNDAMENTALS


Unit II: LOW-POWER DESIGN APPROACHES

Switched Capacitance Minimization Approaches:
System Level Measures, Circuit Level Measures, Mask level Measures.

Unit III: LOW-VOLTAGE LOW-POWER ADDERS

Unit IV: LOW-VOLTAGE LOW-POWER MULTIPLIERS

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

Unit V: LOW-VOLTAGE LOW-POWER MEMORIES


Text Books

2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

Reference Books

Course Code: GR18D5093  

L/T/P/C: 3/0/0/3

Course objectives

- Describe an embedded system design flow from specification to physical realization
- Describe structural behavior of systems.
- Master complex systems.
- Devise new theories, techniques, and tools in design, implementation and testing.
- Master contemporary development techniques.

Course outcomes

- Gain knowledge of contemporary issues and algorithms used.
- Know the interfacing components, different verification techniques and tools.
- Demonstrate practical skills in the construction of prototypes.
- Understand the use of modern hardware and software tools for building prototypes of embedded systems.
- Apply embedded software techniques to satisfy functional and response time requirements.

Unit I: CO-DESIGN ISSUES

Co-Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co-Synthesis Algorithms:
Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

Unit II: PROTOTYPING AND EMULATION

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:
Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.
Unit III: COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

Unit IV: DESIGN SPECIFICATION AND VERIFICATION

Design, co-design, the co-design computational model, concurrency coordinating concurrent Computations, interfacing components, design verification, implementation verification, verification tools, interface verification

Unit V
Languages for System – Level Specification and Design-I:
System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:
Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Text Books


Reference Books

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - springer
Course Code: GR18D5094

L/T/P/C: 0/0/4/2

Course objectives

• To describe overview about evolution of CMOS integrated circuits.
• To provide knowledge about fabrication process and technology
• To introduce and familiarize with the various Amplifiers & OP-amps
• To prepare them to face the challenges in CMOS technology

Course outcomes

• Able to develop an in-depth understanding of the design principles and applications of CMOS analog IC design.
• An ability to know the fabrication steps involved in CMOS technology.
• Familiar with the small signal and large signal models of CMOS transistors.
• An in-depth knowledge of applying the concepts on real time applications.
• Analyze and design of CMOS op Amps and compensation techniques.

Task1
Analyze the NMOS and PMOS Operating point Characteristics.

Task2
Design a CMOS Current Mirror and find out the AC, DC, OP analysis.

Task3
Design a NMOS Differential Amplifier and find out the AC, DC, OP analysis.

Task4
Design a PMOS Differential Amplifier and find out the AC, DC, OP analysis.

Task5
Design a CMOS Operational Amplifier and find out the AC analysis and noise margin analysis.

Task6
Design a comparator using Operational Amplifier and find out the AC analysis.

Task7
Draw the Analog Layout for CMOS current Mirror and perform DRC, LVS, RC Extraction.

Note: All the following digital circuits are to be designed and implemented using Cadence/ Mentor Graphics/ Synopsys/ equivalent CAD Tools.
Task 1
Develop Verification environment using system Verilog for any one digital system.

Task 2
Design and analyze the performance with respect to area, power and speed for different Adders using ASIC Logic Design Tools.

Task 3
Design and analyze the performance with respect to area, power and speed for different Multipliers using ASIC Logic Design Tools.

Task 4
Perform Synthesis for any digital system to meet the given specifications.

Task 5
Perform Static Timing Analysis for any digital system to meet the given specifications.

Task 6
Perform Floor planning, clock tree synthesis, Placement and Routing, RC extraction for given netlist to meet the specifications.

Note: All the following digital circuits are to be designed and implemented using Cadence/ Mentor Graphics/ Synopsys/ equivalent CAD Tools.
Course Code: GR18D5096  L/T/P/C: 3/0/0/3

Course objectives

• To learn how to build the best processor/computing system understanding the underlying tradeoffs and ramifications.
• To identify and analyze the attributes of computer architecture design with recent trend technology.
• To identify the techniques to improve the speed and performance of computers – Parallelism in Instruction level – Hardware approaches – pipelining, dynamic scheduling, superscalar processors, and multiple issue of instructions.
• To implement the design aspects and categorize various issues, causes and hazards due to parallelisms.
• To examine and compare the performance with benchmark standards.

Course outcomes

• An ability to discuss the organization of computer-based systems and how a range of design choices are influenced by applications.
• An ability to understand the components and operation of a memory hierarchy and the range of performance issues influencing its design.
• An ability to interpret the organization and operation of current generation parallel computer systems, including multiprocessor and multicore systems.
• An ability to understand the various techniques to enhance a processors ability to exploit instruction-level parallelism (ILP), and its challenges.
• An ability to undertake performance comparisons of modern and high performance computers.

Unit I: FUNDAMENTALS OF COMPUTER DESIGN

Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl’s law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing type and size of operands, Operations in the instruction set.

Unit II: PIPELINES

Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.  
Unit III: INSTRUCTION LEVEL PARALLELISM (ILP) - THE HARDWARE APPROACH

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo’s approach, Branch prediction, High performance instruction delivery- Hardware based speculation.

**ILP Software Approach:** Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware versus Software.

Unit IV: MULTI PROCESSORS AND THREAD LEVEL PARALLELISM

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

Unit V: INTER CONNECTION AND NETWORKS

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

**Intel Architecture:** Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

**Text Books**


**Reference Books**

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
CAD FOR VLSI

Course Code: GR18D5097  L/T/P/C: 3/0/0/3

Course objectives

- To provide an introduction to the fundamentals of Computer-Aided Design tools for the modelling, design, analysis, test, and verification of digital Very Large Scale Integration (VLSI) systems.
- To study various physical design methods in VLSI.
- To understand the concepts behind the VLSI design rules and routing techniques.
- To use the simulation techniques at various levels in VLSI design flow.
- To understand the concepts of various algorithms used for floor planning and routing techniques.

Course outcome

- Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
- Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
- To practice the application of fundamentals of VLSI technologies
- Optimize the implemented design for area, timing and power by applying suitable constraints.
- To gain knowledge on the methodologies involved in design, verification and implementation of digital designs on reconfigurable hardware platform (FPGA)

Unit I: VLSI PHYSICAL DESIGN AUTOMATION


Unit II: PARTITIONING, FLOOR PLANNING, PIN ASSIGNMENT AND PLACEMENT

Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing, Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments, Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.
Unit III: GLOBAL ROUTING AND DETAILED ROUTING

Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

Unit IV: PHYSICAL DESIGN AUTOMATION OF FPGAS


Physical Design Automation of MCMs
Introduction to MCM Technologies, MCM Physical Design Cycle.

Unit V: CHIP INPUT AND OUTPUT CIRCUITS


Text Books


Reference Books

Course Code: GR18D5098

Course objectives

• This course provides the concepts of switched capacitor circuits used in mixed signal circuit design.
• To know mixed signal circuits like DAC, ADC, PLL etc.,
• To acquire knowledge on design different architectures in mixed signal mode.
• To gain knowledge on noise shaping modulators and higher order modulators.
• It deals with the design and analysis of Biquad Filters.

Course outcomes

• Analyze and design of switched capacitor circuits used in mixed signal circuit design
• Design noise shaping converters given a set of requirements such as bandwidth, clock speed and signal-to-noiseratio
• Design an integrated mixed signal circuit in CMOS using modern design tools
• Demonstrate in-depth knowledge in PLL and Data Converters (DAC and ADC)
• Analyze complex engineering problems critically for conducting research in data converters

Unit I: SWITCHED CAPACITOR CIRCUITS

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

Unit II: PHASED LOCK LOOP (PLL)

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

Unit III: DATA CONVERTER FUNDAMENTALS

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.
Unit IV: NYQUIST RATE A/D CONVERTERS


Unit V: OVERSAMPLING CONVERTERS

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizes, Delta sigma D/A

Text Books


Reference Books

Course Code: GR18D5201  L/T/P/C: 3/0/0/3

Course objectives
- Understand the role of business analytics and statistical tools used within an organization.
- Discuss Trendiness and Regression Analysis and different visualization techniques to explore data.
- Describe the organization structure and different type of business analytics.
- Know Forecasting Techniques, Monte Carlo Simulation and Risk Analysis.
- Understanding decision analysis and recent trends in business intelligence.

Course Outcomes
- Demonstrate business analytics process and use statistical tools for implementation of business process.
- Design relationships and trends to explore and visualize the data.
- Examine the organization structure of business analytics and categorize types of analytics.
- Apply forecasting techniques, monte carlo simulation and risk analysis.
- Formulate decision analysis and summarize recent trends in business intelligence.

Unit I
Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models.

Unit II
Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming.

Unit III
Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

Unit IV
Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

Unit V
Reference Books
INDUSTRIAL SAFETY

Course Code: GR18D5202 L/T/P/C: 3/0/0/3

Course Objectives

- To understand the importance of maintaining a safe workplace.
- To maintain safety standards in compliance with regulatory requirements and within engineering limits understand personal safety and industrial safety.
- To create a job safety analysis (JSA) for a given work project.
- To follow safety recordkeeping and management, and the role of the safety manager.
- To utilize personal proactive equipment.

Course outcomes: After successful completion of the course the student will be able to

- Understanding of safety principles.
- Analyze different types of exposure and biological effects, exposure guidelines and basic workplace monitoring ability to do hazard analysis.
- Demonstrate an understanding of workplace injury prevention, risk management, and incident investigations.
- Understand the acute and chronic health effects of exposure to chemical, physical and biological agents in the workplace.
- Demonstrate knowledge of the types of hazards, planning, organization and training needed to work safely with hazardous materials.

Unit I: INDUSTRIAL SAFETY

Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

Unit II: FUNDAMENTALS OF MAINTENANCE ENGINEERING

Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

Unit III: WEAR AND CORROSION AND THEIR PREVENTION

Unit IV: FAULT TRACING

Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment’s like, I. Any one Machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

Unit V: PERIODIC AND PREVENTIVE MAINTENANCE

Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Reference Books

Course Code: GR18D5203

Course objectives
- To define and formulate linear and non-linear programming problems and appreciate their limitations arising from a wide range of applications.
- To perform sensitivity analysis to determine the direction and magnitude of change of a model’s optimal solution as the data change.
- To distinguish various inventory models and develop proper inventory policies.
- To solve the scheduling and sequencing models.
- To understand how to model and solve problems using dynamic programming, game theory.

Course Outcomes
- The student will formulate and solve problems as networks and graphs for optimal allocation of limited resources such as machine, material and money.
- The student will be able to carry out sensitivity analysis.
- The student will solve network models like the shortest path, minimum spanning tree, and maximum flow problems.
- The student will be able to distinguish various inventory models and develop proper inventory policies.
- The student will also propose the best strategy using decision making methods under uncertainty and game theory.

Unit I
Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models.

Unit II
Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming.

Unit III
Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

Unit IV
Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.
Unit V


Reference Books

Course Objectives

- To provide the student with a clear understanding of strategic cost management process.
- To describe the various stages of project execution.
- To prepare the project schedule by bar charts and network diagram.
- To conduct breakeven and cost-volume-profit analysis.
- To make students various budgets and quantitative techniques used for cost management.

Course outcomes

- The student will be able to explain the various cost concepts used in decision making.
- To be able to identify and demonstrate various stages of project execution.
- The students will be able to prepare the project schedule by bar charts and network diagrams.
- The student will be to differentiate absorption costing and marginal costing, also conduct breakeven and cost-volume-profit analysis.
- The student will be able to prepare various budgets and quantitative techniques used for cost management.

Unit I


Unit II

Project: meaning, Different types, why to manage, cost overruns centers, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and non-technical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

Unit III


**Unit IV**

Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

**Unit V**


**Reference Books**

2. Charles T. Horngren and George Foster, Advanced Management Accounting.
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co.Ltd.
COMPOSITE MATERIALS

Course Code: GR18D5205  L/T/P/C: 3/0/0/3

Course objectives: The objectives of this course is to provide the students,
- To understand the concepts of fundamental science and engineering principles relevant to materials engineering.
- To expose the various methods to test mechanical properties on materials.
- To categorize the various equilibrium diagrams and describe the changes which occurs on metals.
- To explain the concepts on various heat treatment operations.
- To explain the various ferrous and non-ferrous metals with their properties and applications.

Course outcomes: At the end of the course, students will be able to
- Relate crystal structures and identify the relation between different materials.
- Test the various mechanical properties of metal by suitable method.
- Relate the equilibrium transformation diagram for various ferrous and non-ferrous metals.
- Utilize appropriate techniques in treating with proper heat treatment operation.
- Evaluate the behavior of material when it subjected to heat treatment process.

Unit I: INTRODUCTION


Unit II: REINFORCEMENTS


Unit III: MANUFACTURING OF METAL MATRIX COMPOSITES

Unit IV: MANUFACTURING OF POLYMER MATRIX COMPOSITES


Unit V: STRENGTH

Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

Text Books


Reference Books

Course Code: GR18D5206  
L/T/P/C: 3/0/0/3

Course Objectives

- To find or recall the non-hazardous secondary materials from waste.
- To compare precisely to overcome the cost and most economically attractive course of action for CH4 emission.
- To demonstrate the techno-economic feasibility of replacing.
- To extend the students for possible future activity in a biomass plant.
- To utilization in spark-ignited internal combustion engine.

Course outcomes

- Students are able to make use of energy installation and the small of household bio-waste incineration.
- To develop actual dimension must of course, fit requirement of the masonry block.
- To become capable of analyze and design of energy conversion system.
- Students are to estimate the possibility of invest in biomass generation.
- Students will be able to explain the biogas its uses and benefits.

Unit I: INTRODUCTION TO ENERGY FROM WASTE

Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors.

Unit II: BIOMASS PYROLYSIS

Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

Unit III: BIOMASS GASIFICATION

Unit IV: BIOMASS COMBUSTION

Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

Unit V: BIOGAS

Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Reference Books

Course Code: GR18D5207 L/T/P/C: 2/0/0/2

Course objectives
- To state how to put research on paper.
- To demonstrate how to write an abstract.
- To apply the process of research.
- To appraise the key skills involved in writing the title, abstract, introduction and review of literature.
- To compose a paper which is good and has the qualities of acceptance and publication.

Course Outcomes
- Will be able to understand how to write a research paper.
- Will outline the drafting of an abstract.
- Will acquire the skills of various elements of research.
- Will be in a position to write a good paper.
- Will result in increasing the chance of publication.

Unit I
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

Unit II

Unit III
Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

Unit IV
Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature.

Unit V
Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusion.
Reference Books

Course objectives

- Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Critically understand the strengths and weaknesses of disaster management approaches,
- Planning and programming in different countries, particularly their home country or the countries they work in.

Course Outcomes

- Capacity to integrate knowledge and to analyze, evaluate and manage the different public health aspects of disaster events at a local and global levels, even when limited information is available.
- Capacity to describe, analyze and evaluate the environmental, social, cultural, economic, legal and organizational aspects influencing vulnerabilities and capacities to face disasters.
- Capacity to work theoretically and practically in the processes of disaster management (disaster risk reduction, response, and recovery) and relate their interconnections, particularly in the field of the Public Health aspects of the disasters.
- Capacity to manage the Public Health aspects of the disasters.
- Capacity to obtain, analyze, and communicate information on risks, relief needs and lessons learned from earlier disasters in order to formulate strategies for mitigation in future scenarios with the ability to clearly present and discuss their conclusions and the knowledge and arguments behind them.

Unit I: INTRODUCTION

Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Unit II: REPERCUSSIONS OF DISASTERS AND HAZARDS

Unit III: DISASTER PRONE AREAS IN INDIA

Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides and Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics.

Unit IV: DISASTER PREPAREDNESS AND MANAGEMENT

Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.

Unit V: RISK ASSESSMENT


Reference Books

2. Sahni, Pardeep Et.Al. (Eds.),” Disaster Mitigation Experiences and Reflections”, Prentice Hall Of India, NewDelhi.
Course Code: GR18D5209  
L/T/P/C: 2/0/0/2

Course objectives

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world.
- Learning of Sanskrit to improve brain functioning.
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects.
- Enhancing the memory power.
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature.

Course Outcomes

- Understanding basic Sanskrit alphabets and Understand tenses in Sanskrit Language.
- Enable students to understand roots of Sanskrit language.
- Students learn engineering fundamentals in Sanskrit.
- Students can attempt writing sentences in Sanskrit.
- Ancient Sanskrit literature about science & technology can be understood

Unit I
Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences

Unit II
Order, Introduction of roots, Technical information about Sanskrit Literature

Unit III
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

Reference Books

1. “Abhyaspustakam” – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi
2. “Teach Yourself Sanskrit” Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
Course Code: GR18D5201

Course objectives

- Understand value of education and self-development.
- Imbibe good values in students.
- Let the should know about the importance of character.
- To understand the significance of human conduct and self-development.
- To enable students to imbibe and internalize the value and Ethical behaviour in personal and professional lives.

Course outcomes

- Knowledge of self-development.
- Learn the importance of Human values.
- Developing the overall personality.
- Student will be able to realize the significance of ethical human conduct and self-development.
- Students will be able to inculcate positive thinking, dignity of labour and religious tolerance.

Unit I

Values and self-development –Social values and individual attitudes, Work ethics, Indian vision of humanism, Moral and non-moral valuation, Standards and principles, Value judgement.

Unit II


Unit III

Personality and Behavior Development - Soul and Scientific attitude, Positive Thinking, Integrity and discipline, Punctuality, Love and Kindness, Avoid fault Thinking, Free from anger, Dignity of labour, Universal brotherhood and religious tolerance, True friendship, Happiness vs suffering, love for truth, Aware of self-destructive habits, Association and Cooperation, Doing best for saving nature.
Unit IV


Reference Books

Course Code: GR18D5211

Course objectives

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals’ constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.
- To understand the role and functioning of Election Commission of India.

Course outcomes

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.
- Discuss the significance of Election Commission of India.

Unit I: HISTORY OF MAKING OF THE INDIAN CONSTITUTION

History Drafting Committee, (Composition & Working).

Unit II: PHILOSOPHY OF THE INDIAN CONSTITUTION

Preamble Salient Features.

Unit III: CONTOURS OF CONSTITUTIONAL RIGHTS & DUTIES

Unit IV: ORGANS OF GOVERNANCE

Parliament—Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

Unit V: LOCAL ADMINISTRATION


Election Commission: Election Commission: Role and Functioning, Chief Election Commissioner and Election Commissioners, State Election Commission: Role and Functioning, Institute and Bodies for the welfare of SC/ST/OBC and women.

Reference Books

1. The Constitution of India, 1950 (Bare Act), Government Publication.
Course Code: GR18D5212

Course Objectives

- Review existing evidence on the review topic to inform Programme design and policy making.
- Undertaken by the DFID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.
- Establishing coordination among people in order to execute pedagogy methods.
- To study pedagogy as a separate discipline.

Course Outcomes

- What pedagogical practices are being used by teachers in formal classrooms in developing countries?
- What pedagogical practices are being used by teachers in informal classrooms in developing countries?
- Synergy from the work force.
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

Unit I: INTRODUCTION AND METHODOLOGY


Unit II: THEMATIC OVERVIEW

Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

Unit III: EVIDENCE ON THE EFFECTIVENESS OF PEDAGOGICAL PRACTICES

Methodology for the in-depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers’ attitudes and beliefs and Pedagogic strategies.
Unit IV: PROFESSIONAL DEVELOPMENT

Alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community, Curriculum and assessment, Barriers to learning: limited resources and large class sizes.

Unit V: RESEARCH GAPS AND FUTURE DIRECTIONS

Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

Reference Book

Course Code: GR18D5213

Course objectives

- To achieve overall Good Health of Body and Mind.
- To lower blood pressure and improve heart health.
- To become non-violent and truthfulness.
- To increase the levels of happiness.
- To eliminate all types of body pains.

Course outcomes

- Develop healthy mind in a healthy body thus improving social health also improve efficiently.
- Develop body awareness. Learn how to use their bodies in a healthy way. Perform well in sports and academics.
- Will balance, flexibility, and stamina, strengthen muscles and connective tissues enabling good posture.
- Manage stress through breathing, awareness, meditation and healthy movement.
- Build concentration, confidence and positive self-image.

Unit I

Definitions of Eight parts of yog. (Ashtanga)

Unit II

Yam and Niyam. Do’s and Don’t’s inlife. Ahinsa, satya, astheya, bramhacharya andaparigraha Shaucha, santosh, tapa, swadhyay,ishwarpranidhan

Unit III

Asan and Pranayam, Various yog poses and their benefits for mind & body. Regulaization of breathing techniques and its effects-Types of pranayam

Reference Books

1. ‘Yogic Asanas for Group Tarining-Part-I’ : Janardan Swami Yogabhyasi Mandal,Nagpur
2. “Rajayoga or conquering the Internal Nature” by SwamiVivekananda, Advaita Ashrama (Publication Department),Kolkata
Course Code: GR18D5214

Course objectives

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students
- To differentiate three types of happiness (Sukham)
- To describe the character traits of a spiritual devotee

Course outcomes

- Study of Shrimad- Bhagwad-Gita will help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- To develop self-developing attitude towards work without self-aggrandizement
- To develop tranquil attitude in all favorable and unfavorable situations
- To develop high spiritual intelligence

Unit I: Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)
- Verses- 52,53,59 (don’ts)
- Verses- 71,73,75,78 (do’s)

Unit II: Approach to day to day work and duties.

- Shrimad Bhagwad Geeta: Chapter 2-Verses 41,47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23,35,
- Chapter 18-Verses 45, 46,48.

Unit III: Statements of basic knowledge.

- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62,68
- Chapter 12 -Verses 13, 14, 15, 16,17,18
- Personality of Role model. Shrimad BhagwadGeeta: Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18,38,39
- Chapter18 – Verses 37,38,63
**Reference Books**

1. “Srimad Bhagavad Gita” by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata
2. Bhartrihari’s Three Satakam (Niti-sringar-vairagya) by P. Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.