ACADEMIC REGULATIONS
PROGRAM STRUCTURE
and
DETAILED SYLLABUS

Master of Technology
(VLSI)

(Two Year Regular Programme)
(Applicable for the Batches admitted from 2014)

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
(Autonomous)

Gokaraju Rangaraju
Institute of Engineering and Technology, Hyderabad
M. Tech. GR14 Regulations

Gokaraju Rangaraju Institute of Engineering & Technology 2014 Regulations (GR14 Regulations) are given hereunder. These regulations govern the programmes offered by the Department of Electronics Communication and Engineering with effect from the students admitted to the programmes in 2014-15 academic year.

1. **Programme Offered:** The programme offered by the Department is M.Tech in VLSI, a two-year regular programme.

2. **Medium of Instruction:** The medium of instruction (including examinations and reports) is English.

3. **Admissions:** Admission to the M.Tech in VLSI Programme shall be made subject to the eligibility, qualifications and specialization prescribed by the Institute/University from time to time. Admissions shall be made either on the basis of the merit rank obtained by the student in PGECET conducted by the APSCHE for M. Tech Programmes or on the basis of any other order of merit approved by the University, subject to reservations as prescribed by the Government from time to time.

4. **Programme Pattern:**
   a) Each Academic year of study is divided into two semesters.
   b) Minimum number of instruction days in each semester is 90.
   c) The total credits for the Programme is 88.
   d) All the registered credits will be considered for the calculation of the final percentage of marks.

5. **Award of M.Tech Degree:** A student will be declared eligible for the award of the M. Tech Degree if he/she fulfills the following academic requirements:
   a) A student shall be declared eligible for the award of M.Tech degree, if he/she pursues the course of study and completes it successfully in not less than two academic years and not more than four academic years.
   b) A Student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the date of admission, shall forfeit his/her seat in M.Tech course.
   c) The Degree of M.Tech in VLSI shall be conferred by Jawaharlal Nehru Technological University Hyderabad (JNTUH), Hyderabad, on the students who are admitted to the programme and fulfill all the requirements for the award of the degree.

6. Attendance Requirements

a) A student shall be eligible to appear for the end semester examinations if he/she puts in a minimum of 75% of attendance in aggregate in all the courses concerned in the semester.

b) Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in a semester may be granted. A committee headed by Dean (Academic Affairs) shall be the deciding authority for granting the condonation.

c) Students who have been granted condonation shall pay a fee as decided by the Academic Council.

d) A candidate shall get minimum required attendance at least in three (3) heory subjects in the semester to get promoted to the next semester. In order to qualify for the award of M.Tech Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.

e) Students whose shortage of attendance is not condoned in any semester are detained and are not eligible to take their end examinations of that semester. They may seek re-registration for that semester when offered next with the academic regulations of the batch into which he/she gets re-registered.

7. Paper Setting, Evaluation of Answer Scripts, Marks and Assessment

a) Paper setting and Evaluation of the Answer Scripts shall be done as per the procedures laid down by the Academic Council of the College from time to time.

b) The following is the division of marks between internal and external evaluations.

Particulars	Internal	External	Total
Theory	40	60	100
Practical	40	60	100
Comprehensive Viva	--	100	100
Seminar	50	----	50
Project Work	Grade	-----	----
Project work & dissertation (Grading System)	------	Grade	----

c) Continuous Internal Evaluation and Semester End Examinations

The assessment of the student's performance in each course will be based on continuous internal evaluation and semester-end examinations. The marks for each of the component of assessment are fixed as shown in the following Table.

Assessment Procedure

S.No	Component of Assessment	Marks Allotted	Type of Assessment	Scheme of Examinations
1	Theory	40	Internal Exams & Continuous Evaluation	1. Mid-examinations: … 30 Marks (Two mid-semester examinations shall be conducted for 30 marks each for duration of 2 hours. Average of the two mid semester examinations shall be considered) 2. Tutorial: … … 5 Marks 3. Attendance: .. 5 Marks
		60	Semester-end examination	The semester-end examination is for a duration of 3 hours
2	Practical	40	Internal Exams & Continuous Evaluation	1) Lab Internal :15 marks 2) Record : 5 marks 3) Continuous Assessment : 15 marks 4) Attendance : 5 marks
		60	Semester-end examination	The semester-end examination is for a duration of 3 hours.

D) Comprehensive Viva: There shall be a Comprehensive Viva-Voce in II year I semester. The Comprehensive Viva-Voce will be conducted by the committee consisting of Head of the Department and two senior faculty members of the Department. The Comprehensive Viva-Voce is aimed to assess the student's understanding in various subjects he/she studies during the M.Tech course of study. The Comprehensive Viva-Voce is valued for 100 marks by the committee. There are no internal marks for the Comprehensive Viva-voce.

e) Seminar: There shall be three Seminar Presentations by the student, one each in the I, II and III semesters. For the seminar, the student shall collect the information on a specialized topic other than his/her project and prepare a technical report, showing his understanding over the topic, and

submit to the department, which shall be evaluated by a Departmental committee consisting of the Head of the department, seminar Supervisor and a senior faculty member. The seminar report shall be evaluated for 50 marks. There shall be no external examination for seminar.

f) Project: The work on the project shall be initiated in the beginning of the second year and the duration of the project is for two semesters (III & IV). Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the Project Review Committee (PRC).
   i) PRC shall be constituted with HOD as chair person, two senior faculty members and project supervisor.
   ii) Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects (theory and practical subjects).
   iii) A candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the PRC for its approval. Only after obtaining the approval of PRC the student can initiate the Project work.
   iv) If a candidate wishes to change his supervisor or topic of the project he/she can do so with approval of PRC. However, the PRC shall examine whether the change of topic/supervisor leads to a major change of his initial plans of project proposal. If so, his date of registration for the project work starts from the date of change of supervisor or topic as the case may be.
   v) Project Work: The candidate should be continuously observed by the project supervisor. His performance is assessed by the PRC through a seminar and interim report. Full credits are awarded 'SAT' on satisfactory performance of the student. 'US' grade is given on unsatisfactory performance. If the performance is unsatisfactory, the PRC should redefined the project and the candidate is allowed to appear for the evaluation only after six months.
   vi) Project Work & Dissertation: A candidate shall submit status report (in a bound-form) in two stages at least with a gap of 3 months between them to the project supervisor.
   vii) A candidate is permitted to submit Project dissertation only after successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of dissertation to the Head of the Department and shall make an oral presentation before the PRC along with project supervisor.
   viii) Student has to submit to the department three copies of the Project dissertation along with a soft copy on CD certified by the supervisor.
   ix) The dissertation shall be adjudicated by one examiner selected by the Controller of examination from the panel of 3 examiners as suggested

by Head of the Department, who are eminent in that field with the help of the concerned guide and head of the department.

x) If the report of the Examiner is not favorable, the candidate shall revise and resubmit the dissertation, in the time frame as described by PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected.

xi) If the report of the examiner is favorable, viva-voce examination shall be conducted by a board consisting of the supervisor, Head of the Department and the examiner who adjudicated the dissertation. The Board shall jointly report candidates work as:
A. Excellent
B. Good
C. Satisfactory
D. Unsatisfactory

Head of the Department shall coordinate and make arrangements for the conduct of viva-voce examination.

If the report of the viva-voce is unsatisfactory, the candidate will retake the viva-voce examination after three months. If he/she fails to get a satisfactory report at the second viva-voce examination, he/she will not be eligible for the award of the degree.

8. **Recounting of Marks in the End Examination Answer Books:** A student can request for re-counting of his/her answer book on payment of a prescribed fee.

9. **Re-evaluation of the End Examination Answer Books:** A student can request for re-evaluation of his/her answer book on payment of a prescribed fee.

10. **Supplementary Examinations:** A student who has failed in an end semester examination can appear for a supplementary examination, as per the schedule announced by the College/Institute.

11. **Malpractices in Examinations:** Disciplinary action shall be taken in case of malpractices during Mid/ End-examinations as per the rules framed by the Academic Council.

12. **Academic Requirements:**
    a) A student shall be deemed to have secured the minimum academic requirements in a subject if he / she secures a minimum of 40% of marks in the Semester-end Examination and a minimum aggregate of 50% of the total marks in the Semester-end examination and Internal Evaluation taken together.

b) In order to qualify for the award of M.Tech Degree, the student shall complete the academic requirements of passing in all the Courses as per the course structure including Seminars and Project if any.

c) In case a Student does not secure the minimum academic requirements in any course, he/she has to reappear for the Semester-end Examination in the course, or re-register for the same course when next offered or re-register for any other specified course, as may be required. However, one more additional chance may be provided for each student, for improving the internal marks provided the internal marks secured by a student are less than 50% and he/she failed finally in the course concerned. In the event of taking another chance for re-registration, both the internal and external marks obtained in the previous attempt are nullified. In case of re-registration, the student has to pay the re-registration fee for each course, when next offered.

13. **Award of Class:** After a student satisfies all the requirements prescribed for the completion of the Degree and becomes eligible for the award of M. Tech Degree by JNTUH, he/she shall be placed in one of the following three classes:

Class Awarded	% of Marks Secured
First Class with Distinction	Marks ≥ 70%
First Class	60% ≤ Marks < 70%
Second Class	50% ≤ Marks < 60%

14. **Withholding of Results:** If the student has not paid dues to the Institute/ University, or if any case of indiscipline is pending against him, the result of the student (for that Semester) may be withheld and he/she will not be allowed to go into the next Semester. The award or issue of the Degree may also be withheld in such cases.

15. **Transfer of students from the Constituent Colleges of JNTUH or from other Colleges/ Universities:** Transfer of students from the Constituent Colleges of JNTUH or from other Colleges/ Universities shall be considered only on case-to-case basis by the Academic Council of the Institute.

16. **Transitory Regulations:** Students who have discontinued or have been detained for want of attendance, or who have failed after having undergone the Degree Programme, may be considered eligible for re-registration to the same or equivalent subjects as and when they are offered.

17. General Rules

a) The academic regulations should be read as a whole for the purpose of any interpretation.
b) In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Academic Council is final.
c) In case of any error in the above rules and regulations, the decision of the Academic Council is final.
d) The college may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the Institute/ University.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
M.TECH (VLSI)

VLSI - M.Tech - I Year, I Semester

Group	Sub-Code	Subject	Credits	Int	Ext	Marks
PC	GR14D5077	VLSI Technology and Design	3	40	60	100
PC	GR14D5094	CMOS Analog Integrated Circuit Design	3	40	60	100
PC	GR14D5086	CPLD & FPGA Architectures & Applications	3	40	60	100
PC	GR14D5095	CMOS Digital Integrated Circuit Design	3	40	60	100
		Elective I	3	40	60	100
PE	GR14D5079	Digital System Design				
	GR14D5083	Hardware Software Co-Design				
	GR14D5096	Device Modeling				
		Elective II	3	40	60	100
PE	GR14D5081	Advanced Operating Systems				
	GR14D5073	Microcontrollers for Embedded System				
	GR14D5096	Design Advanced Computer Architecture				
LAB	GR14D5097	VLSI Lab I	2	40	60	100
SPW	GR14D5175	Seminar-I	2	—	—	—
		Total	**22**	**280**	**420**	**700**

VLSI - M.Tech- I Year, II Semester

Group	Sub-Code	Subject	Credits	Int	Ext	Marks
PC	GR14D5098	Low Power VLSI Design	3	40	60	100
PC	GR14D5099	CAD for VLSI Circuits	3	40	60	100
PC	GR14D5100	CMOS Mixed Signal Circuit Design	3	40	60	100
PC	GR14D5101	Design for Testability	3	40	60	100
		Elective III	3	40	60	100
PE	GR14D5102	Scripting Language				
	GR14D5103	Digital Signal Processors and Architectures				
	GR14D5104	VLSI Signal Processing				
		Elective IV	3	40	60	100
PE	GR14D5105	Optimization Techniques in VLSI Design				
	GR14D5106	System On Chip Architecture				
	GR14D5107	Semiconductor Memory Design and Testing				
LAB	GR14D5108	VLSI Lab II	2	40	60	100
SPW	GR14D5176	Seminar-II	2	—	—	—
		Total	**22**	**280**	**420**	**700**

VLSI - M.Tech - II Year, I Semester

Group	Sub-Code	Subject	Credits	Int	Ext	Marks
SPW	GR14D5178	Comprehensive Viva	2	—	100	100
SPW	GR14D5177	Seminar-III	2	50	—	50
SPW	GR14D5179	Project work	18	Grade		
		Total	**22**	**50**	**100**	**150**

VLSI - M.Tech - II Year, II Semester

Group	Sub-Code	Subject	Credits	Int	Ext	Marks
SPW	GR14D5180	Project work and Dissertation	22	Grade		

I-Year

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

VLSI TECHNOLOGY AND DESIGN

Course Code: GR14D5077 L:3 T:0 P:0 C:3
I Year I Semester

Unit-I
Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

Unit-II
Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.
Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

Unit-III
Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

Unit-IV
Sequential Systems: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

Unit-V
Floor Planning: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

Text Books
1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

Reference Books
1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

CMOS ANALOG INTEGRATED CIRCUIT DESIGN

Course Code: GR14D5094 L:3 T:0 P:0 C:3
I Year I Semester

Unit-I
MOS Devices and Modeling: The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

Unit-II
Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

Unit-III
CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

Unit-IV
CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

Unit-V
Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop
Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Text Books

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

Reference Books

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

Course Code: GR14D5086 L:3 T:0 P:0 C:3
I Year I Semester

Unit-I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

Unit-II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

Unit-III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

Unit-IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

Unit-V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Text Books

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

Reference Books

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

Course Code: GR14D5095 L:3 T:0 P:0 C:3
I Year I Semester

Unit-I
MOS Design: Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

Unit-II
Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

Unit-III
Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

Unit-IV
Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

Unit-V
Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

Text Books
1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici TMH, 3rd Ed., 2011.

Reference Books

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
ELECTIVE -I
DIGITAL SYSTEM DESIGN

Course Code: GR14D5079 L:3 T:0 P:0 C:3
I Year I Semester

Unit-I

Minimization and Transformation of Sequential Machines: The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.
Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

Unit-II

Digital Design: Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner,
Binary divider.

Unit-III

SM Charts: State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

Unit-IV

Fault Modeling & Test Pattern Generation: Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model. Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

Unit-V

Fault Diagnosis in Sequential Circuits: Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

Text Books

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design Miron Abramovici, Melvin A.
3. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
4. Logic Design Theory – N. N. Biswas, PHI

Reference Books

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
ELECTIVE I
HARDWARE - SOFTWARE CO-DESIGN

Course Code: GR14D5083 L:3 T:0 P:0 C:3
I Year I Semester

Unit-I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co synthesis.

Unit-II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Unit-III

Compilation Techniques & Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

Unit-IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

Unit-V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Text Books

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

Reference Book

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 –Springer

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
ELECTIVE I
DEVICE MODELLING

Course Code: GR14D5096 L:3 T:0 P:0 C:3
I Year I Semester

Unit-I

Introduction to Semiconductor Physics: Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.
Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

Unit-II

Integrated Diodes: Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models
Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon modeldynamic model, Parasitic effects – SPICE model –Parameter extraction

Unit-III

Integrated MOS Transistor: NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

Unit-IV

VLSI Fabrication Techniques: An overview of wafer fabrication, Wafer Processing – Oxidation –Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements –Interconnects circuit elements

Unit-V

Modeling of Hetero Junction Devices: Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

Text Books

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

Reference Books

1. Physics of Semiconductor Devices – Sze S. M, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
ELECTIVE II
ADVANCED OPERATING SYSTEMS

Course Code: GR14D5081 L:3 T:0 P:0 C:3
I Year I Semester

Unit-I

Introduction to Operating Systems: Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

Unit-II

Introduction to UNIX and LINUX: Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations

Unit-III

System Calls: System calls and related file structures, Input / Output, Process creation & termination.

Inter Process Communication: Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams &
Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

Unit-IV

Introduction to Distributed Systems: Goals of distributed system, Hardware and software concepts, Design issues.

Communication in Distributed Systems: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

Unit-V

Synchronization in Distributed Systems: Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions

Deadlocks: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

Text Books

1. The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete Reference LINUX Richard Peterson, 4th Ed., McGraw Hill.

Reference Books

1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems - Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles - Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
ELECTIVE -II
MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

Course Code: GR14D5073 L:3 T:0 P:0 C:3
I Year I Semester

Unit-I

ARM Architecture: ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

Unit-II

ARM Programming Model-I: Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

Unit –III

ARM Programming Model-II: Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

Unit-IV

ARM Programming: Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

Unit-V

Memory Management: Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

Text Book

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

Reference Book

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
ELECTIVE -II
ADVANCED COMPUTER ARCHITECTURE

Course Code: GR14D5096 L:3 T:0 P:0 C:3
I Year I Semester

Unit-I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing type and size of operands, Operations in the instruction set.

Unit-II

Pipelines: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

Unit-III

Instruction Level Parallelism (ILP) - The Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation.

ILP Software Approach: Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

Unit-IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

Unit-V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

Text Book

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

Reference Books

1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

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VLSI LABORATORY-I

Course Code: GR14D5097 L:3 T:0 P:0 C:3
I Year I Semester

Note: All the following digital circuits are to be designed and implemented using Cadence /Mentor Graphics / Synopsys / Equivalent CAD tools.

VLSI Front End Design programs
Programming can be done using any HDL complier, Verification of the Functionality of the module using functional Simulator, Timing Simulation for Critical Path time Calculation, Synthesis of module, Place & Route and implementation of design using FPGA/CPLD Devices.

1. HDL code to realize all the logic gates
2. Design and Simulation of Half and Full adders, Serial Binary Adder, Multi Precision Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with priority)
5. Design of 8-to-1 multiplexer and 1x8 De multiplexer
6. Design of 4 bit binary to gray code converter
7. Design of 4-bit comparator.
8. Design of flip flops: SR, D, JK, T.
9. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset).
10. Design of a N- bit shift register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
11. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
12. Design of 4- Bit Multiplier and 4-bit Divider.
13. Design of ALU to Perform – ADD, SUB, AND, OR, 1's compliment, 2's Compliment, Multiplication and Division.
14. Design of Finite State Machine.

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LOW POWER VLSI DESIGN

Course Code: GR14D5098 L:3 T:0 P:0 C:3
I Year II Semester

Unit-I

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

Unit-II

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

Unit-III

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

Unit-IV

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

Unit-V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Text Books

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

Reference Books

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.

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CAD FOR VLSI CIRCUITS

Course Code: GR14D5099 L:3 T:0 P:0 C:3
I Year II Semester

Unit-I

VLSI Physical Design Automation: VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles;

Unit-II

Partitioning, Floor Planning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing, Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments, Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms;

Unit-III

Global Routing and Detailed Routing: Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms;

Unit-IV

Physical Design Automation of FPGAs: FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model;
Physical Design Automation of MCMs: Introduction to MCM Technologies, MCM Physical Design Cycle.

Unit-V

Chip Input and Output Circuits: ESD Protection, Input Circuits, Output Circuits and noise, On-chip clock Generation and Distribution, Latch-up and its prevention.

Text Books

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

GOKARAJU RANGARAJU
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CMOS MIXED SIGNAL CIRCUIT DESIGN

Course Code: GR14D5100 L:3 T:0 P:0 C:3
I Year II Semester

Unit-I
Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

Unit-II
Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

Unit-III
Data Converter Fundamentals: DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

Unit-IV
Nyquist Rate A/D Converters: Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

Unit-V
Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

Text Books
1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

Reference Books

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

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DESIGN FOR TESTABILITY

Course Code: GR14D5101 L:3 T:0 P:0 C:3
I Year II Semester

Unit-I
Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

Unit-II
Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

Unit-III
Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

Unit-IV
Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

Unit-V
Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Text Books
1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

Reference Books
1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
ELECTIVE -III
SCRIPTING LANGUAGES

Course Code: GR14D5102 L:3 T:0 P:0 C:3
I Year II Semester

Unit-I

Introduction to Scripts and Scripting: Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

Unit-II

Advanced Perl: Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

Unit-III

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

Unit-IV

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

Unit-V

TK and JavaScript: Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Pythan.

Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

Text Books

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.

2. Practical Programming in Tcl and Tk - Brent Welch, Ken Jones and Jeff Hobbs., Fourth edition.
3. Java the Complete Reference - Herbert Schildt, 7th Edition, TMH.

Reference Books

1. Tcl/Tk: A Developer's Guide- Clif Flynt, 2003, Morgan Kaufmann SerieS.
2. Tcl and the Tk Toolkit- John Ousterhout, 2nd Edition, 2009, Kindel Edition.
3. Tcl 8.5 Network Programming book- Wojciech Kocjan and Piotr Beltowski, Pack Publishing.

GOKARAJU RANGARAJU
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ELECTIVE -III
DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

Course Code: GR14D5103 L:3 T:0 P:0 C:3
I Year II Semester

Unit-I

Introduction to Digital Signal Processing: Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

Unit-II

Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Unit-III

Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

Unit-IV

Analog Devices Family of DSP Devices: Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

Unit-V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

Text Books

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

Reference Books

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
ELECTIVE -III
VLSI SIGNAL PROCESSING

Course Code: GR14D5104 L:3 T:0 P:0 C:3
I Year II Semester

Unit-I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

Unit-II

Folding and Unfolding: Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems

Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

Unit-III

Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

Unit-IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic

Convolution – Design of Fast Convolution algorithm by Inspection

Unit-V

Low Power Design: Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

Text Books

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

Reference Books

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

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ELECTIVE -IV
OPTIMIZATION TECHNIQUES IN VLSI DESIGN

Course Code: GR14D5105 L:3 T:0 P:0 C:3
I Year II Semester

Unit-I

Statistical Modeling: Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgroms model, Principle component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

Unit-II

Statistical Performance, Power and Yield Analysis Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

Unit-III

Convex Optimization: Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

Unit-IV

Genetic Algorithm: Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation-partitioning-automatic placement, routing technology, Mapping for FPGA-Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement-GASP algorithm-unified algorithm.

Unit-V

GA Routing Procedures and Power Estimation: Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA-Standard cell placement-GA for ATGproblem encoding- fitness function-GA Vs Conventional algorithm.

Text Books / Reference Books

1. Statistical Analysis and Optimization for VLSI: Timing and Power - Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation - Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998.
3. Convex Optimization - Stephen Boyd, Lieven Vandenberghe, Cambridge University Press, 2004.

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ELECTIVE -IV
SYSTEM ON CHIP ARCHITECTURE

Course Code: GR14D5106 L:3 T:0 P:0 C:3
I Year II Semester

Unit-I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

Unit-II

Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

Unit-III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

Unit-IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.

Unit-V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

Text Books

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely IndiaPvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

Reference Books

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
ELECTIVE -IV
SEMICONDUCTOR MEMORY DESIGN AND TESTING

Course Code: GR14D5107 L:3 T:0 P:0 C:3
I Year II Semester

Unit-I

Random Access Memory Technologies: SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM

Unit-II

Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

Unit-III

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

Unit-IV

Semiconductor Memory Reliability and Radiation Effects: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

Unit-V

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories,

magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

Text Books

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K.Sharma- 2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
ELECTIVE -IV
VLSI LABORATORY II

Course Code: GR14D5058 L:3 T:0 P:0 C:3
I Year II Semester

Note: All the following digital/analog circuits are to be designed and implemented using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.
The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

VLSI Back End Design programs:

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:

- CMOS inverter
- CMOS NOR/ NAND gates
- CMOS XOR and MUX gates
- CMOS half adder and full adder
  Static / Dynamic logic circuits (register cell) Latch Pass transistor

3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths
4. Introduction to SPICE simulation and coding of NMOS/CMOS circuit
5. SPICE simulation of basic analog circuits: Inverter / Differential amplifier
6. Analog Circuit simulation (AC analysis) CS & CD amplifier
7. System level design using PLL