

ACADEMIC REGULATIONS PROGRAM STRUCTURE and DETAILED SYLLABUS

Master of Technology

[VLSI]

(Two Year Regular Programme)

(Applicable for Batches admitted from 2015)



**GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY**

(Autonomous)



ACADEMIC REGULATIONS

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

For all Postgraduate Programmes (M.Tech)
GR15 REGULATIONS

Gokaraju Rangaraju Institute of Engineering & Technology-2015 Regulations (GR 15 Regulations) are given hereunder. These regulations govern all the Post Graduate programmes offered by various departments of Engineering with effect from the students admitted to the programmes from 2015-16 academic year.

1. **Programme Offered:** The Post Graduate programme offered by the department is M.Tech, a two-year regular programme in that discipline.
2. **Medium of Instruction:** The medium of instruction (including examinations and reports) is English.
3. **Admissions:** Admission into the M.Tech Programme in any discipline shall be made subject to the eligibility and qualifications prescribed by the University from time to time. Admissions shall be made either on the basis of the merit rank obtained by the student in PG CET conducted by the APS CHE for M. Tech Programmes or on the basis of any other order of merit approved by the University, subject to reservations as prescribed by the Government from time to time.
4. **Programme Pattern:**
 - a) A student is introduced to “Choice Based Credit System (CBCS)” for which he/she has to register for the courses at the beginning of each semesters as per the procedure.
 - b) Each Academic year of study is divided into two semesters.
 - c) Minimum number of instruction days in each semester is 90.
 - d) The total credits for the Programme is 88.
 - e) Grade points, based on percentage of marks awarded for each course will form the basis for calculation of SGPA (Semester Grade Point Average) and CGPA (Cumulative Grade Point Average).
 - f) A student has a choice of registering for credits from the courses offered in the programme.
 - g) All the registered credits will be considered for the calculation of final CGPA.
5. **Award of M.TechDegree:** A student will be declared eligible for the award of the M. Tech Degree if he/she fulfills the following academic requirements:
 - a) A student shall be declared eligible for the award of M.Tech degree, if he/she pursues the course of study and completes it successfully in not less than two academic years and not more than four academic years.



- B) A Student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the date of admission, shall forfeit his/her seat in M.Tech courses.
- c) The Degree of M.Tech shall be conferred by Jawaharlal Nehru Technological University Hyderabad (JNTUH), Hyderabad, on the students who are admitted to the programme and fulfill all the requirements for the award of the degree.

6. Attendance Requirements

- a) A student shall be eligible to appear for the semester end examinations if he/she puts in a minimum of 75% of attendance in aggregate in all the courses concerned in the semester.
- b) Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in a semester may be granted. A committee headed by Dean (Academic Affairs) shall be the deciding authority for granting the condonation.
- c) Students who have been granted condonation shall pay a fee as decided by the Academic Council.
- d) A candidate shall get minimum required attendance at least in three theory subjects in the semester to get promoted to the next semester. In order to qualify for the award of M.Tech. Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.
- E) Students whose shortage of attendance is not condoned in any semester are detained and are not eligible to take their end examinations of that semester. They may seek re-registration for that semester when offered next with the academic regulations of the batch into which he/she gets re-registered.

7. Paper Setting, Evaluation of Answer Scripts, Marks and Assessment

- a) Paper setting and Evaluation of the Answer Scripts shall be done as per the procedures laid down by the Academic Council of the College from time to time.
- b) The following is the division of marks between internal and external evaluations.

S.no	Particulars	Internal	External	Total
1	Theory	30	70	100
2	Practical	30	70	100
3	Comprehensive Viva	-	100	100
4	Seminar	30	70	100
5	Project work	30	70	100

- c) The marks for internal evaluation per semester per theory course are divided as follows:
- i. **For Mid written examinations: 20 Marks**
 - ii. **For Assignment: 5 Marks**
 - iii. **For Attendance: 5 Marks**
 - iv. **Total: 30Marks**
- d) **Mid-Term Written Examination:** There shall be two mid-term written examinations during a semester. The first mid-term written examination shall be conducted from the first



50 per cent of the syllabus and the second mid-term written examination shall be conducted from the remaining 50 per cent of the syllabus. The mid-term written examinations shall be evaluated for **20 marks** and average of the marks scored in the two mid-term written examinations shall be taken as the marks scored by each student in the mid-term written examination for that semester.

- e) **Assignment:** Assignments are to be given to the students and marks not exceeding 5 (5%) per semester per paper are to be awarded by the teacher concerned.
- f) **Attendance:** A maximum of 5 marks (5%) per semester per course are to be awarded on the basis of attendance one puts in. Course-wise attendance is taken for this purpose.
- g) **For Internal Evaluation in Practical/Lab Subjects:** The marks for internal evaluation are 30. Internal Evaluation is done by the teacher concerned with the help of the other staff member nominated by Head of the Department. Marks Distribution is as follows:
- | | |
|---|-----------------|
| i. Writing the program/Procedure: | 10 Marks |
| ii. Executing the program/Procedure: | 10 Marks |
| iii. Viva: | 05 Marks |
| iv. Attendance: | 05 Marks |
| v. Total: | 30Marks |
- h) **For External Evaluation in Practical/Lab Subjects:** The Semester end examination shall be conducted by an external examiner and a staff member of the Department nominated by Head of the Department. Marks distribution is as follows:
- | | |
|---|-----------------|
| i. Writing the program/Procedure: | 20 Marks |
| ii. Executing the program/Procedure: | 20 Marks |
| iii. Viva: | 15 Marks |
| iv. Lab Record: | 15 Marks |
| v. Total: | 70 Marks |
- i) **Evaluation of Main Project Work:** A Project Review Committee (PRC) is to be constituted by the Principal/Director with Head of the Department as the Chairman and two other senior faculty members of the department.
- i. **Registration for Project work:** A candidate is permitted to register for the project work after satisfying the attendance requirements of all the courses (theory and practical courses) up to III Semester.
- ii. After satisfying the registration requirements, a candidate is permitted to register for the project work after satisfying, the title, objectives and plan of action of his project work to the Project Review Committee for its approval. Only after obtaining the approval of Project Review Committee of the Department, the student can initiate the project work. Any changes thereafter in the project are to be approved by PRC. The student has to work under the guidance of both internal guide (one faculty member of the department) and external guide (from Industry not below the rank of an officer). Internal guide is allotted by the Head of the Department or Coordinator of the Project Work whereas external guide is allotted by the industrial organization in which the project is undertaken.
- iii. The candidate shall submit status of the report in two stages at least with a gap of 20 days between them.



- iv. The work on the project shall be initiated in the beginning of the fourth semester and the duration is one semester. A candidate is permitted to submit project report only after successful completion of theory and practical courses with the approval of PRC and not earlier than 40 days from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of the thesis to the Head/Coordinator (through internal research guide) and shall make an oral presentation before the PRC.
- v. Two hardcopies and one soft copy of the project work (dissertation) certified by the research supervisors shall be submitted to the College/Institute.
- vi. The thesis shall be adjudicated by one external examiner selected by the Institute out of 5-member panel, submitted by the department.
- vii. The marks allotted for project work review are 100, out of which 30 are for internal and 70 for external. Internal evaluation marks are awarded by the PRC on the basis of the student's performance in the three pre-submission reviews and the external evaluation is done by the external examiner.
- viii. The marks allotted for project work and dissertation are 100, out of which 30 are for internal and 70 for external. Internal evaluation marks are awarded by the PRC on the basis of the student's performance in the three pre-submission reviews and the external evaluation is done by the external examiner. In both internal and external evaluations the student shall score at least 40% marks and an aggregate of 50% marks to pass in the project work. If the report of the examiner is favorable, Viva-voce examination shall be conducted by a Board consisting of the Supervisor, Head and the External Examiner who adjudicated the project work. The Board shall jointly evaluate the student's performance in the project work.
- ix. In case the student doesn't pass through the project work, he has to reappear for the viva-voce examination, as per the recommendations of the Board. If he fails to succeed at the second Viva-voce examination also, he will not be eligible for the award of the degree, unless he is asked to revise and resubmit the Project by the Board. Head of the Department and Project coordinator shall coordinate and make arrangements for the conduct of viva-voce examination. When one does get the required minimum marks both in internal and external evaluations the candidate has to revise and resubmit the dissertation in the time frame prescribed by the PRC. If the report of the examiner is unfavorable again, the project shall be summarily rejected.
- x. If the report of the viva-voce is not satisfactory, the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination, he will not be eligible for the award of the degree, unless the candidate is asked to revise and resubmit.

8. **Recounting of Marks in the End Examination Answer Books:** A student can request for re-counting of his/her answer book on payment of a prescribed fee.
9. **Re-evaluation of the End Examination Answer Books:** A student can request for re-evaluation of his/her answer book on payment of a prescribed fee.
10. **Supplementary Examinations:** A student who has failed in an end semester examination can appear for a supplementary examination, as per the schedule announced by the College/Institute.



11. Malpractices in Examinations: Disciplinary action shall be taken in case of malpractices during Mid/ End-examinations as per the rules framed by the Academic Council.

12. Academic Requirements

- a) A student shall be deemed to have secured the minimum academic requirement in a subject if he / she secures a minimum of 40% of marks in the Semester-end Examination and a minimum aggregate of 50% of the total marks in the Semester-end examination and Internal Evaluation taken together.
 - b) A student shall be promoted to the next semester only when he/she satisfies the requirements of all the previous semesters.
 - c) In order to qualify for the award of M.Tech Degree, the student shall complete the academic requirements of passing in all the Courses as per the course structure including Seminars and Project if any.
 - d) In case a Student does not secure the minimum academic requirement in any course, he/she has to reappear for the Semester-end Examination in the course, or re-register for the same course when next offered or re-register for any other specified course, as may be required. However, one more additional chance may be provided for each student, for improving the internal marks provided the internal marks secured by a student are less than 50% and he/she failed finally in the course concerned. In the event of taking another chance for re-registration, the internal marks obtained in the previous attempt are nullified. In case of re-registration, the student has to pay the re-registration fee for each course, as specified by the College.
- E) Grade Points:** A 10- point grading system with corresponding letter grades and percentage of marks, as given below, is followed

Letter Grade	Grade Point	Percentage of Marks
O (Outstanding)	10	Marks \geq 80 and Marks \leq 100
A+ (Excellent)	9	Marks \geq 70 and Marks $<$ 80
A (Very Good)	8	Marks \geq 60 and Marks $<$ 70
B+ (Good)	7	Marks \geq 55 and Marks $<$ 60
B (Above Average)	6	Marks \geq 50 and Marks $<$ 55
F (Fail)	0	Marks $<$ 50
Ab (Absent)	0	

Earning of Credit:

A student shall be considered to have completed a course successfully and earned the credits if he/she secures an acceptable letter grade in the range O-P. Letter grade 'F' in any Course implies failure of the student in that course and no credits earned.

Computation of SGPA and CGPA:

The UGC recommends the following procedure to compute the Semester Grade Point



Average (SGPA) and Cumulative Grade Point Average (CGPA):

- i) S_k the SGPA of k th semester (1 to 4) is the ratio of sum of the product of the number of credits and grade points to the total credits of all courses registered by a student,

$$SGPA (S_k) = \frac{\sum_{i=1}^n (C_i \cdot G_i)}{\sum_{i=1}^n C_i}$$

Where C_i is the number of credits of the i th course and G_i is the grade point scored by the student in the i th course and n is the number of courses registered in that semester.

- ii) The CGPA is calculated in the same manner taking into account all the courses m , registered by a student over all the semesters of a programme, i.e., upto and inclusive of S_k , where $k \geq 2$.

$$CGPA = \frac{\sum_{i=1}^m (C_i \cdot G_i)}{\sum_{i=1}^m C_i}$$

- iii) The SGPA and CGPA shall be rounded off to 2 decimal points.

- 13. Award of Class:** After a student satisfies all the requirements prescribed for the completion of the Degree and becomes eligible for the award of M. Tech Degree by JNTUH, he/she shall be placed in one of the following four classes:

	Class Awarded	CGPA Secured
3.1	First class with distinction	CGPA > 7.75
3.2	First Class	CGPA > 6.75 and CGPA < 7.75
3.3	Second Class	CGPA \geq 6.00 and CGPA < 6.75

- 14. Withholding of Results:** If the student has not paid dues to the Institute/ University, or if any case of indiscipline is pending against him, the result of the student (for that Semester) may be withheld and he will not be allowed to go into the next Semester. The award or issue of the Degree may also be withheld in such cases.

- 15. Transfer of students from the Constituent Colleges of JNTUH or from other Colleges/ Universities:** Transfer of students from the Constituent Colleges of JNTUH or from other Colleges/ Universities shall be considered only on case-to-case basis by the Academic Council of the Institute.

- 16. Transitory Regulations:** Students who have discontinued or have been detained for want of attendance, or who have failed after having undergone the Degree Programme, may be considered eligible for readmission to the same or equivalent subjects as and when they are offered.

17. General Rules

- The academic regulations should be read as a whole for the purpose of any interpretation.
- In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Academic Council is final.
- In case of any error in the above rules and regulations, the decision of the Academic Council is final.
- The college may change or amend the academic regulations or syllabi at any time and the



changes or amendments made shall be applicable to all the students with effect from the dates notified by the college.





GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

M.Tech (VLSI) PROGRAMME STRUCTURE

M.Tech (VLSI)

I Year-I Semester

Sub-Code	Group	Subject	L	P	C	Int.	Ext.	Total
GR15D5077	PC	VLSI Technology and Design	4	0	4	30	70	100
GR15D5094	PC	CMOS Analog Integrated Circuit Design	4	0	4	30	70	100
GR15D5086	PC	CPLD & FPGA Architectures and Applications	4	0	4	30	70	100
	OE-I	Open Elective – I	4	0	4	30	70	100
	Elective I							
GR15D5079	PE	Digital System Design	4	0	4	30	70	100
GR15D5102	PE	Scripting Languages for VLSI						
GR15D5096	PE	Device Modelling						
	Elective II							
GR15D5081	PE	Advanced Operating Systems	4	0	4	30	70	100
GR15D5073	PE	Micro Controllers for Embedded Systems Design						
GR15D5095	PE	CMOS Digital Integrated Circuit Design						
GR15D5097	Lab	VLSI Lab – I	0	4	2	30	70	100
GR15D5173	SPW	Seminar – I	-	4	2	30	70	100
		Total Credits	28	6	24	240	560	800

M.Tech (VLSI)

I Year-II Semester

Sub-Code	Group	Subject	L	P	C	Int.	Ext.	Total
GR15D5099	PC	CAD for VLSI Circuits	4	0	4	30	70	100
GR15D5100	PC	CMOS Mixed Signal Circuit Design	4	0	4	30	70	100
GR15D5101	PC	Design for Testability	4	0	4	30	70	100
	OE – II	Open Elective – II	4	0	4	30	70	100
	Elective III							
GR15D5098	PE	Low Power VLSI Design	4	0	4	30	70	100
GR15D5084	PE	Digital Signal Processors & Architectures						
GR15D5103	PE	VLSI Signal Processing						
	Elective IV							
GR15D5104	PE	Optimization Techniques in VLSI Design	4	0	4	30	70	100
GR15D5091	PE	System On Chip Architecture						
GR15D5105	PE	Semiconductor Memory Design & Testing						
GR15D5106	Lab	VLSI Lab – II	0	4	2	30	70	100
GR15D5174	SPW	Seminar – II	-	4	2	30	70	100
		Total	24	8	28	240	560	800



II Year-I Semester

Sub-Code	Group	Subject	L	P	C	Int.	Ext.	Total
GR15D5175	SPW	Comprehensive Viva-voce	-	-	4	0	100	100
GR15D5176	SPW	Project work Review	-	-	12	30	70	100
Total			-	-	16	30	170	200

II Year-II Semester

Sub-Code	Group	Subject	L	P	C	Int.	Ext.	Total
GR15D5177	SPW	Project work and Dissertation	-	-	16	30	70	100
Total					16	30	70	100

A student has a choice to select one Open Elective Pool I in I Semester and one Open Elective Pool II in II Semester.

Open Elective Pool-I

Sub-Code	Group	Subject	L	P	C	Int.	Ext.	Total
GR15D5178	OE-I	E- Commerce and Applications (CSE)	4	0	4	30	70	100
GR15D5179		Enterprise Resource Planning (IT)	4	0	4	30	70	100
GR15D5180		Modern Control Theory (EEE)	4	0	4	30	70	100
GR15D5181		Computer - Oriented Numerical Methods in Engineering (CE)	4	0	4	30	70	100
GR15D5182		Advanced Computer Architecture (ECE)	4	0	4	30	70	100
GR15D5183		Operations Research (ME)	4	0	4	30	70	100

Open Elective Pool-II

Sub-Code	Group	Subject	L	P	C	Int.	Ext.	Total
GR15D5184	OE-II	Human Computer Interaction (CSE)	4	0	4	30	70	100
GR15D5185		Big Data and Analytics (IT)	4	0	4	30	70	100
GR15D5186		Neural and Fuzzy Systems (EEE)	4	0	4	30	70	100
GR15D5187		Project Management (CE)	4	0	4	30	70	100
GR15D5188		Hardware Software Co-Design(ECE)	4	0	4	30	70	100
GR15D5189		Non-Conventional Energy Resources(ME)	4	0	4	30	70	100



I- SEMESTER







GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
VLSI TECHNOLOGY AND DESIGN

M.Tech (VLSI)
Course Code: GR15D5077

I Year - I Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To enable the student to visualize MOS fabrication technologies and to understand electrical properties of MOS, CMOS and Bi CMOS circuits.
- To train the student to draw integrated circuit layouts following design rules.
- To enable the student design combinational circuit, do verification, power optimization and network testing.
- To enable the student to use power optimization techniques, design validation procedures and testing of sequential circuits.
- To train the student to use different floor planning methods and different low power architectures.

COURSE OUTCOMES: Graduate student will be able to

- Visualize the steps taken for MOS fabrication technologies.
- Analyze electrical behavior of MOS, CMOS and Bi CMOS circuits.
- Draw the layout of integrated circuits following design rules.
- Design combinational circuit.
- Design sequential circuits using different clocking disciplines.
- Carry out power optimization techniques, design validation procedure and testing of circuits.
- Carry out floor planning for different low power architectures.

UNIT-I

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: $I_{ds} - V_{ds}$ relationships, Threshold Voltage V_T , G_m , G_{ds} and ω_0 , Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Z_{pu}/Z_{pd} , MOSTransistor circuit model, Latch-up in CMOS circuits.

UNIT-II

Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.



UNIT-III

Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT-IV

Sequential Systems: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT-V

Floor Planning: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, D. A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principles of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
CMOS ANALOG INTEGRATED CIRCUIT DESIGN

M.Tech (VLSI)
Course Code: GR15D5094

I Year - I Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To describe over view about evolution of CMOS integrated circuits.
- To provide knowledge about fabrication process and technology
- To introduce and familiarize with the various Amplifiers & OP-amps
- To prepare them to face the challenges in CMOS technology

COURSE OUTCOMES: After going through this course the student will be able to

- Able to develop an in-depth understanding of the design principles and applications of CMOS analog IC design
- An ability to know the fabrication steps involved in CMOS technology.
- Familiar with the small signal and large signal models of CMOS transistors
- An in-depth knowledge of applying the concepts on real time applications
- Analyze and design of CMOS op Amps and compensation techniques
- Analyze the basic current mirrors and understand voltage references
- An ability to understand the basic concepts of CMOS technology and its simulation models

UNIT -I

MOS Devices and Modeling: The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II:

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III:

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV:

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of



Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OPAMP.

UNIT -V:

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

M.Tech (VLSI)
Course Code: GR15D5086

I Year - I Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To understand the concept of Programmable Logic Device architectures and technologies.
- Underlying FPGA architectures and technologies in detail.
- To understand the difference between CPLDs and FPGAs
- To provide knowledge about SRAM Programmable FPGA Device architecture.
- To comprehend knowledge about Anti-Fuse Programmable FPGA Device architecture.
- To furnish knowledge about various applications of FPGA.
- To provide knowledge about FPGA based case studies.

COURSE OUTCOMES: After going through this course the student will be able to

- To know the concept of programmable architectures.
- Perceiving CPLD and FPGA technologies
- Study and compare the different architectures of CPLDs and FPGAs
- An ability to know the SRAM Technology based FPGAs
- An ability to know the Anti-Fuse Technology based FPGAs
- Design and impose applications using FPGAs.
- Construct a digital system using FPGA.

UNIT-I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable LogicArrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; ComplexProgrammable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLDImplementation of a Parallel Adder with Accumulation.

UNIT-II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures,Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated SpecializedComponents of FPGAs, Applications of FPGAs.

UNIT -III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 andXC4000 Architectures.



UNIT -IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, TheActel ACT1, ACT2 and ACT3Architectures.

UNIT -V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a RobotManipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders andAccumulators with the ACT Architecture.

TEXT BOOKS

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

DIGITAL SYSTEM DESIGN
(Elective -I)

M.Tech (VLSI)
Course Code: GR15D5079

I Year - I Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- Learn digital design of Sequential Machines.
- Learn drawing state graphs.
- Learn realization and implementation of SM Charts.
- Learn Fault modeling and test pattern generation of Combinational circuits.
- Learn fault diagnosis in sequential circuits and understand machine design, identification of fault detection experiment.

COURSE OUTCOMES: After going through the course students will be able to

- Create understanding of the design techniques of sequential Machines.
- Create understanding of the fundamental concepts of PLD's, design of FPGA's.
- Learn implementation of SM charts in combinational and sequential circuits.
- Develop skills in modeling fault free combinational circuits.
- Develop skills in modeling Sequential circuits in terms of reliability, availability and safety.
- Develop skills in modeling fault detection experiments of sequential circuits.
- Develop skills in modeling combinational circuits in terms of reliability, availability and safety.

UNIT-I

Minimization and Transformation of Sequential Machines: The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT-II:

Digital Design: Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT-III:

SM Charts: State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

**UNIT-IV:**

Fault Modeling & Test Pattern Generation: Logic Fault model – Fault detection & Redundancy-Fault equivalence and fault location –Faultdominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Randomtesting, Transition count testing, Signature analysis and test bridging faults.

UNIT-V

Fault Diagnosis in Sequential Circuits: Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – MironAbramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

SCRIPTING LANGUAGES FOR VLSI
(Elective -I)

M.Tech (VLSI)
Course Code: GR15D5102

I Year - I Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To describe the need of using scripting language programs.
- To use PERL scripting language at the instances required.
- To apply advanced level PERL for software automation.
- To employ the PERL scripting language for file system navigation.
- To illustrate software automation using TCL
- To apply TCL for event-driven programs.
- To describe PERL-TK, Java Scripts, and basics of python languages.

COURSE OUTCOMES: After going through this course the student will be able to

- The students will be in a position to judge whether scripting language program is needed for a particular code.
- Students will be acquainted with the basic level scripting language programming in PERL.
- Students will be skillful to code in PERL for advanced level software automation.
- Students will be having capability to code for file system navigation.
- Students will be calibre to code for software automation using TCL scripting language.
- Students will have the programming skills to automate the software for event-driven programs too.
- Students will be in a position to demonstrate software automation using Java Script, PERL-TK, and in basic level using python scripting language.

UNIT -I

Introduction to Scripts and Scriptings: Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT -II

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the filesystem, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.



UNIT -III

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT -IV

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

UNIT -V

TK and JavaScript: Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK, JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python. Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

TEXT BOOKS

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Practical Programming in Tcl and Tk - Brent Welch, Ken Jones and Jeff Hobbs., Fourth edition.
3. Java the Complete Reference - Herbert Schildt, 7th Edition, TMH.

REFERENCE BOOKS

1. Tcl/Tk: A Developer's Guide- Clif Flynt, 2003, Morgan Kaufmann Series.
2. Tcl and the Tk Toolkit- John Ousterhout, 2nd Edition, 2009, Kindle Edition.
3. Tcl 8.5 Network Programming book- Wojciech Kocjan and Piotr Beltowski, Packt Publishing.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

DEVICE MODELLING
(Elective-I)

M.Tech (VLSI)
Course Code: GR15D5096

I Year - I Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To impart to students knowledge of semi conductor physics and integrated passive devices.
- To enable students to analyze the behavior of monolithic diodes with the help of models of integrated diodes.
- To enable students to analyze the behavior of integrated NMOS and PMOS transistors with the help of SPICE models.
- To enable students visualize different VLSI fabrication techniques of different processes.
- To enable students to model hetero junction devices.

COURSE OUTCOMES

- The graduate student will be equipped with knowledge of semiconductor physics.
- The graduate student will be able relate model parameters to structures of integrated passive devices.
- The graduate will be able to analyze static and dynamic behavior of diodes.
- The graduate student will be able to model electrically NMOS and PMOS transistors.
- The graduate student will be able to use SPICE model level 1, 2,3 and 4 and hence will be able to analyze various integrated circuits.
- The graduate student will have sound knowledge of VLSI fabrication technique details of different processes.
- The graduate student will be able to model electrically hetero junction devices.

UNIT-I

Introduction to Semiconductor Physics: Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.

Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

UNIT -II

Integrated Diodes:

Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models

Integrated Bipolar Transistor:

Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gummel - Poon model dynamic model, Parasitic effects – SPICE model –Parameter extraction

**UNIT-III:**

Integrated MOS Transistor: NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics– MOS FET SPICE model level 1, 2, 3 and 4

UNIT -IV

VLSI Fabrication Techniques: An overview of wafer fabrication, Wafer Processing – Oxidation –Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements

UNIT-V

Modeling of Hetero Junction Devices: Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

TEXT BOOKS

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCE BOOKS

1. Physics of Semiconductor Devices – Sze S. M, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRCPress, 2011



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

ADVANCED OPERATING SYSTEMS
(Elective -II)

M.Tech (VLSI)
Course Code: GR15D5081

I Year - I Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To learn the fundamentals, purpose, structure and functions of operating systems.
- To understand how the operating system abstractions can be used in the development of application programs, or to build higher level abstractions.
- To gain insight on to the distributed resource management components viz. the algorithms for implementation of distributed shared memory and commit protocols.
- To gain knowledge on Distributed operating system concepts that includes architecture, Mutual exclusion algorithms.
- To explain how to characterize and cope with processor deadlock, including prevention, avoidance, detection, and recovery.
- To know the components and management aspects of Real time, Mobile operating systems.
- To provide experience in low-level systems programming in a realistic development environment.

COURSE OUTCOMES: After going through this course the student will be able to

- An ability to describe the basic principles used in the design of modern operating systems.
- An ability to understand the difference between different types of modern operating systems, virtual machines and their structure of implementation and applications.
- An ability to understand the difference between process & thread and use of locks, semaphores, monitors for synchronizing multiprogramming with multithreaded systems.
- An ability to distinguish between various resource management techniques for distributed systems.
- An ability to understand the concepts of deadlock in operating systems and how they can be managed / avoided and implement them in multiprogramming system.
- An ability to identify the different features of real time and mobile operating systems.
- An ability to modify existing open source kernels in terms of functionality or features used.

UNIT-I

Introduction to Operating Systems: Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System



UNIT-II

Introduction to UNIX and LINUX: Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations

UNIT-III

System Calls: System calls and related file structures, Input / Output, Process creation & termination.

Inter Process Communication: Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT-IV

Introduction to Distributed Systems: Goals of distributed system, Hardware and software concepts, Design issues.

Communication in Distributed Systems: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT-V

Synchronization in Distributed Systems: Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions

Deadlocks: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS

1. The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete Reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill.

REFERENCE BOOKS

1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems - Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles - Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

MICROCONTROLLERS FOR EMBEDDED SYSTEM
DESIGN (Elective-II)

M.Tech (VLSI)
Course Code: GR15D5073

I Year - I Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To introduce the outline architecture of ARM7 microcontroller including basics of pipelines, registers, exception modes.
- To set up and customize a microcontroller development environment.
- To give an overview of system peripherals which cover bus structure, memory map, register programming and much more.
- To write programs that interact with other devices.
- To learn the Memory Management of RISC Microcontrollers.

COURSE OUTCOMES: After going through this course the student will be able to

- An ability to understand the hardware implementation of the ARM7 microcontrollers.
- An ability to Integrate peripherals based on I/O functions.
- An ability to learn the concept of pipelines, registers and exception modes
- An ability to program in ARM and THUMB modes.
- An ability to interpret the functions of Memory Management Unit (MMU).
- An ability to compare the performance of various ARM families of Microcontrollers.
- An ability to know the software development flow and working with projects.

UNIT-I

ARM Architecture: ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT-II

ARM Programming Model – I: Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT-III

ARM Programming Model-II: Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT-IV

ARM Programming: Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.



UNIT-V

Memory Management: Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N.Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes/ Cole, 1999, Thomas Learning.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

CMOS DIGITAL INTEGRATED CIRCUIT
DESIGN (Elective -II)

M.Tech (VLSI)
Course Code: GR15D5095

I Year - I Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To describe over view about evolution of CMOS integrated circuits.
- To provide knowledge about Combinational, Sequential MOS logic circuits
- To introduce and familiarize with the various logic circuits.
- To prepare them to face the challenges in dynamic logic circuits.
- To prepare them to design various building blocks in combinational and sequential circuits.
- To create interest in the integrated circuit design and prepare them to face .the challenges in VLSI technology.
- An understanding of engineering and management principles and apply these to manage project.

COURSE OUTCOMES: After going through this course the student will be able to

- An ability to know about the various Combinational and Sequential MOS logic circuits.
- An in-depth knowledge of applying the concepts on real time applications
- An ability to know the design of dynamic MOS logic circuits.
- Able to know the design of semiconductor memories.
- An ability to understand the basic concepts of Boolean expressions.
- Able to design different Combinational logic blocks.
- Able to analyze and implement various memory elements.

UNIT-I

MOS Design: Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III

Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip flop.



UNIT-IV

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

VLSI LAB – I

M.Tech (VLSI)
Course Code: GR15D5097

I Year - I Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To learn the logic design of Digital circuits.
- To learn implementation of designs using Hardware description language.
- To learn the concept of timing simulation
- To learn implementation of RTL codes using various simulation tools.
- To learn CAD tools for design and implementation using FPGA and CPLD devices.
- To learn Test pattern generation for Digital circuits.
- To learn the implementation of placement and routing using CAD Tools

Course Outcomes: After going through the course students will be able to

- Gain knowledge in Design of logic designs.
- Know to write HDL codes for all digital designs and implement using simulation tools.
- Know obtaining timing simulation, calculating performance analysis.
- Know the implementation of physical design techniques.
- Know the implementation of design in FPGA and CPLD Devices
- Synthesize combinational and sequential designs
- Implementation of physical design.

Note: All the following digital circuits are to be designed and implemented using Cadence /Mentor Graphics / Synopsys / Equivalent CAD tools.

VLSI Front End Design programs: Programming can be done using any HDL compiler, Verification of the Functionality of the module using functional Simulator, Timing Simulation for Critical Path time Calculation, Synthesis of module, Place & Route and implementation of design using FPGA/CPLD Devices.

1. HDL code to realize all the logic gates
2. Design and Simulation of Half and Full adders, Serial Binary Adder, Multi Precision Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with priority)
5. Design of 8-to-1 multiplexer and 1x8 De-multiplexer
6. Design of 4 bit binary to gray code converter
7. Design of 4-bit comparator
8. Design of flip flops: SR, D, JK, T
9. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset).



10. Design of a N- bit shift register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
11. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
12. Design of 4- Bit Multiplier and 4-bit Divider.
13. Design of ALU to Perform – ADD, SUB, AND, OR, 1's compliment, 2's Compliment, Multiplication and Division.
14. Design of Finite State Machine.



OPEN ELECTIVE - I





GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

E - COMMERCE AND APPLICATIONS
(Open Elective I)

M.Tech (CSE)
 Course Code: GR15D5178

I Year - I Semester
 L/P/C: 4/0/4

Course Objectives

- To understand the interest and opportunity of e-commerce
- To know and understand the critical success factors in implementing an ecommerce System
- To know how to plan and how to manage e-commerce solutions
- To have hands on, real-life experience with electronic commerce applications
- To analyze and understand the human, technological and business environment
- Associated with e-commerce

Course Outcomes: At the end of the course, the student will be able to

- Understand the trends in e-Commerce and the use of the Internet.(Level 2)
- Analyze, Understand and Compare the principles of E-commerce and basics of World Wide Web.(Level 2&4)
- Analyze, Understand the concept of electronic data interchange and its legal, social and technical aspects.(Level 2&4)
- Understand and Evaluate the security issues over the web, the available solutions and future aspects of e-commerce security .(Level 2&5)
- Understanding and Validating the concept of E-banking, electronic payment system.(Level 2&5)
- Understand, Analyze and Compare the capabilities and limitation of agents, Web based marketing and various security Issues. (Level 2&4)
- Understanding and Evaluation of online advertisements, website design issues and Creating a business transaction using an e commerce site.(Level 2,5 &6)

UNIT-I

INTRODUCTION Traditional commerce and E commerce – Internet and WWW – role of WWW – value chains – strategic business and Industry value chains – role of E commerce, advantages of E commerce, anatomy of e commerce applications.

UNIT-II

INFRASTRUCTURE FOR E COMMERCE Packet switched networks – TCP/IP protocol script – Internet utility programmes – SGML, HTML and XML – web client and servers – Web client/server architecture – intranet and extranets.



UNIT-III

WEB BASED TOOLS FOR E COMMERCE Web server – performance evaluation - web server software feature sets – web server software and tools – web protocol – search engines – intelligent agents –EC software – web hosting – cost analysis

UNIT- IV

SECURITY Computer security classification – copy right and Intellectual property – electronic commerce threats – protecting client computers – electronic payment systems and risks involved in it –electronic cash __ micro payment system– strategies for marketing – sales and promotion – cryptography –authentication.

UNIT-V

INTELLIGENT AGENTS Definition and capabilities – limitation of agents – security – web based marketing – search engines and Directory registration – online advertisements – Portables and info mechanics – website design issues.

TEXT BOOKS

1. Ravi Kalakota, “ Electronic Commerce”, Pearson Education,
2. Gary P Schneider “Electronic commerce”, Thomson learning & James T Peny Cambridge USA, 2001.

REFERENCES BOOK

1. EfraimTurvanJ.Lee, David kug and chung, “Electronic commerce” Pearson Education Asia 2001.
2. Brenda Kienew E commerce Business Prentice Hall, 2001.
3. Manlyn Greenstein and Miklos “Electronic commerce” McGraw-Hill, 2002.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

ENTERPRISE RESOURCE PLANNING
(Open Elective-I)

M.Tech (IT)

Course Code: GR15D5179

I Year - I Semester

L/P/C: 4/0/4

PREREQUISITES

- Fundamentals of enterprise resource planning (ERP) systems concepts
- Importance of integrated information systems in an organization.

COURSE OBJECTIVES: The objective of the course is to provide the student

- Understanding of the basic concepts of ERP systems for manufacturing or service companies, and the differences among MRP, MRP II, and ERP systems
- Thinking in ERP systems: the principles of ERP systems, their major components, and the relationships among these components
- Capability to adapt in-depth knowledge of major ERP components, including material requirements planning, master production scheduling, and capacity requirements planning
- Understanding knowledge of typical ERP systems, and the advantages and limitations of implementing such systems
- Understanding the business process of an enterprise
- Grasp the activities of ERP project management cycle
- Understanding the emerging trends in ERP developments

COURSE OUTCOMES: At the end of the course the student will be able to

- Examine systematically the planning mechanisms in an enterprise, and identify all components in an ERP system and the relationships among the components
- Understand production planning in an ERP system, and systematically develop plans for an enterprise
- Use methods to determine the correct purchasing quantity and right time to buy an item, and apply these methods to material management
- Understand the difficulties of a manufacturing execution system, select a suitable performance measure for different objectives, and apply priority rules to shop floor control
- Knowledge of ERP implementation cycle
- Awareness of core and extended modules of ERP
- Apply emerging trends in ERP

UNIT-I

Introduction: Overview – Benefits of ERP – ERP and Related Technologies – Business Process Reengineering – Data Warehousing – Data Mining – On-line Analytical Processing – Supply Chain Management.

**UNIT-II**

IMPLEMENTATION: Implementation Life Cycle – Implementation Methodology – Hidden Costs – Organizing Implementation – Vendors, Consultants and Users – Contracts – Project Management and Monitoring.

UNIT- III

BUSINESS MODULES: Business Modules in an ERP Package – Finance – Manufacturing – Human Resource – Plant Maintenance – Materials Management – Quality Management – Sales and Distribution.

UNIT- IV

ERP MARKET: ERP Market Place – SAP AG – PeopleSoft – Baan Company – JD Edwards World Solutions Company – Oracle Corporation – QAD – System Software Associates.

UNIT- V

ERP-Present and future : Turbo Charge the ERP System – EIA – ERP and E-Commerce – ERP and Internet – Future Directions in ERP.

TEXT BOOKS

1. Alexis Leon, "ERP Demystified", Tata McGraw Hill, 1999.
2. Joseph A. Brady, Ellen F. Monk, Bret J. Wangner, "Concepts in Enterprise Resource Planning", Thomson Learning, 2001.
3. Vinod Kumar Garg and N.K .Venkata Krishnan, "Enterprise Resource Planning – concepts and Planning", Prentice Hall, 1998.
4. Jose Antonio Fernandz, " The SAP R /3 Hand book", Tata McGraw Hill



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

MODERN CONTROL THEORY
(Open Elective-I)

M.Tech (EEE)
Course Code: GR15D5180

I Year - I Semester
L/P/C: 4/0/4

PREREQUISITE: Control Systems, Mathematics.

COURSE OBJECTIVES

- To familiarize students with the modelling of systems
- To familiarize the students with the state space analysis of dynamic systems and observe their controllability and Observability.
- To make students understand the concepts of describing function analysis of nonlinear systems and analyze the stability of the systems.
- To analyze the stability of the nonlinear systems.

COURSE OUTCOMES

- Ability to obtain the mathematical model of any system.
- Ability to obtain the state model for dynamic systems.
- Ability to analyze the controllability and Observability for various types of control systems.
- Ability to understand the various types of nonlinearity.
- Ability to analyze the stability of the nonlinear systems.
- Ability to synthesize the nonlinear systems.

UNIT-I

MATHEMATICAL PRELIMINARIES: Fields, Vectors, Vector Spaces — Linear combinations and Bases — Linear Transformations and Matrices — Scalar Product and Norms ,Eigenvalues, Eigen Vectors and a Canonical form representation of linear operators, The concept of state — State Equations for Dynamic systems, Time invariance and Linearity Non uniqueness of state model — State diagrams for Continuous-Time State models.

UNIT-II

STATE VARIABLE ANALYSIS: linear Continuous time models for Physical systems-- Existence and Uniqueness of Solutions to Continuous- time State Equations — Solutions of Linear Time Invariant Continuous-Time State Equations—State transition matrix and it's properties.

CONTROLLABILITY AND OBSERVABILITY-General concept of controllability— General concept of Observability—Controllability tests for Continuous-Time Invariant Systems --- Observability tests for Continuous-Time Invariant Systems— Controllability and Observability of State Model in Jordan Canonical form— Controllability and Observability Canonical forms of State model.

**UNIT- III****NON LINEAR SYSTEMS -I**

Introduction to Non Linear Systems - Types of Non-Linearities-Saturation-Dead-Zone - Backlash Jump Phenomenon etc;— Singular Points-Introduction to Linearization of nonlinear systems, Properties of Non Linear systems-Describing function-describing function analysis of nonlinear systems-Stability analysis of Non-Linear systems through describing functions.

UNIT-IV**NON LINEAR SYSTEMS-II**

Introduction to phase-plane analysis, Method of Isoclines for Constructing Trajectories, singular points, phase- plane analysis of nonlinear control systems.

UNIT-V**STABILITY ANALYSIS**

Stability in the sense of Lyapunov, Lyapunovs stability and Lyapunov's instability theorems - Stability Analysis of the Linear continuous time invariant systems by Lyapunov second method — Generation of Lyapunov functions Variable gradient method — Krasooviski's method.

TEACHING METHODOLOGIES

1. White board
2. PPTs
3. Seminars

EXT BOOKS

1. Modern Control System Theory by M.Gopal — New Age International -1999
2. Modern Control Engineering by Ogata:K — Prentice Hall – 1997

REFERENCE BOOK

1. Control Systems Engineering, N. S. Nise: 4th Ed., Wiley, 2004.Engineering, 4th Ed., Wiley, 2004.



GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

COMPUTER-ORIENTED NUMERICAL METHODS IN ENGINEERING

(Open Elective-I)

M.Tech (Civil)

Course Code: GR15D5181

I Year - I Semester

L/P/C: 4/0/4

COURSE OBJECTIVES

- To develop the skill of solving linear algebraic systems by direct and iteration methods.
- To illustrate advanced matrix techniques in the determination of Eigen values and Eigen vectors of square matrix.
- To analyze the performance of various interpolation technique and perform error analysis.
- To compare various numerical differentiation and integration techniques.
- To explain the various techniques to study Initial and Boundary value problems in ODE.
- To solve a range of problems on applicable software.

COURSE OUT COMES: At the end of the course the student will be able to

- Solve linear algebraic system by direct and iteration methods.
- Apply the knowledge of Eigen values and Eigen vectors to some contents in engineering.
- Develop the skill of working with symmetric matrices in the study of Engineering problems.
- Apply the knowledge of interpolation and extrapolation of uniform and non uniform data to certain contents of Civil Engineering.
- Apply the knowledge of numerical differentiation and integration to some contents of Civil Engineering
- Learn grid based methods to solve Initial and Boundary value problems that arise in engineering problems.
- Develop the skill of solving computational problems using software.

UNIT-I

Solutions of linear equations: Direct method – Cramer’s rule, Gauss – Elimination method- Gauss Jordan elimination – Triangulation (LU Decomposition) method – Iterative methods Jacobi – Iteration method – Gauss – Seidel iteration, Successive over –relaxation method.

Eigen values and eigen vectors: Jacobi method for symmetric matrices- Given’s method for symmetric matrices-Householder’s method for symmetric matrices-Rutishauser method of arbitrary matrices –Power method.*Demonstration of solutions using open source software in Numerical Methods.

UNIT-II

Interpolation: Linear Interpolation - Higher order Interpolation - Lagrange Interpolation – Interpolating polynomials using finites differences- Hermite Interpolation -piece-wise and spline Interpolation.*Demonstration of solutions using open source software in Numerical methods.



UNIT - III

Finite Difference and their Applications: Introduction- Differentiation formulas by Interpolating parabolas – Backward and forward and central differences- Derivation of Differentiation formulae using Taylor series- Boundary conditions- Beam deflection – Solution of characteristic value problems- Richardson's extrapolation- Use of unevenly spaced pivotal points- Integration formulae by interpolating parabolas- Numerical solution to spatial differential equations. *Demonstration of solutions using open source software in Numerical Methods.

UNIT-IV

Numerical Differentiation: Difference methods based on undetermined coefficients- optimum choice of step length– Partial differentiation. Numerical Integration: Method based on interpolation-method based on undetermined coefficient – Gauss – Lagrange interpolation method- Radaua integration method- composite integration method – Double integration using Trapezoidal and Simpson's method.*Demonstration of solutions using open source software in Numerical Methods.

UNIT-V

Ordinary Differential Equation: Euler's method – Backward Euler method – Mid point method – single step method, Taylor's series method- Boundary value problems-case studies. *Demonstration of solutions using open source software in Numerical Methods.

***NOTE:** Demonstration of solutions using open source software in Numerical Methods only for the knowledge of students to apply in their Project Works. Not for examination.

TEXT BOOKS

1. M.K.Jain-S.R.K.Iyengar, R.K.Jain Numerical methods for scientific and engineering computations, Willey Eastern Limited, 1987
2. S.S.Shastry, Numerical methods.
3. Curtis I.Gerala, Applied numerical analysis, Addison Wasley published campus.

REFERENCES BOOKS

1. C.Chopra, Raymond P.Canal, Numerical methods for Engineers Stevan, Mc. Graw Hill book Company, 4th edition, 2002.
2. C.Xavier, C Language and Numerical methods, New age international publisher, 2003.
3. Dr. M.Shanta Kumar, Computer based numerical analysis, Khanna Book publishers, New Delhi.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

ADVANCED COMPUTER ARCHITECTURE
(Open Elective-I)

M.Tech (ECE)
Course Code: GR15D5182

I Year - I Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To learn how to build the best processor/computing system understanding the underlying tradeoffs and ramifications.
- To identify and analyze the attributes of computer architecture design with recent trend technology.
- To identify the techniques to improve the speed and performance of computers – Parallelism in Instruction level – Hardware approaches - pipelining, dynamic scheduling, superscalar processors, and multiple issue of instructions.
- To implement the design aspects and categorize various issues , causes and hazards due to parallelisms.
- To examine and compare the performance with benchmark standards.
- To understand the framework for evaluating design decisions in terms of application requirements and performance measurements.
- To learn the design and analysis of complex and high performance multiprocessors and supporting subsystems from the quantitative aspect.

COURSE OUTCOMES: After going through this course the student will be able to

- An ability to discuss the organisation of computer-based systems and how a range of design choices are influenced by applications.
- An ability to understand the components and operation of a memory hierarchy and the range of performance issues influencing its design.
- An ability to interpret the organisation and operation of current generation parallel computer systems, including multiprocessor and multicore systems.
- An ability to understand the various techniques to enhance a processors ability to exploit instruction-level parallelism (ILP), and its challenges.
- An ability to know the classes of computers, and new trends and developments in computer architecture.
- An ability to develop the applications for high performance computing systems.
- An ability to undertake performance comparisons of modern and high performance computers.

UNIT -I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law.



Instruction set principles and examples- Introduction, classifying instruction set- memory addressing type and size of operands, Operations in the instruction set.

UNIT-II

Pipelines: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT-III

Instruction Level Parallelism (ILP) - The Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation.

ILP Software Approach:

Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT-IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism-Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT-V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS

1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

OPERATIONS RESEARCH
(Open Elective-I)

Mtech(ME)

Course Code: GR15D5183

I Year - I Semester

L/P/C: 4/0/4

COURSE OBJECTIVES: The Objective of this course is to provide

- Analysis of quantitative methods and techniques for effective Decision-making.
- Constructing models that are used in solving business decision problems.
- Introduce the students to the use of basic methodology for the solution of linear programs and integer programs.
- Introduce the students to methods for solving large-scale transportation and assignment problems.
- Illustrate how sequencing is carried out in assigning jobs to machines
- Understand the concept of Inventory and apply different models in optimizing the same.
- Apply PERT/CPM: [Project scheduling and allocation of resources] to schedule and control construction of dams, bridges, roads etc. in an optimal way.

COURSE OUTCOMES: At the end of the course, the student will be able to:

- Apply various linear programming techniques for optimal allocation of limited resources such as machine, materials and money
- Solve transportation problems to minimize cost and understand the principles of assignment of jobs and recruitment policies.
- Solve game theory problems.
- Solve problems of inventory and develop proper inventory policies.
- Apply PERT/CPM: [Project scheduling and allocation of resources] to schedule and control construction of dams, bridges, roads etc in a optimal way.
- Solve sequencing problems.
- Develop optimum replacement policy

UNIT-I

Introduction: Definition and scope of operations research(OR),ORmodel, solving the OR model, art of modeling, phases of OR study.

Linear Programming:

Two variable Linear Programming model and Graphical method of solution, Simplex method, Dual Simplex method, special cases of Linear Programming, duality, sensitivity analysis.

UNIT-II

Transportation Problems: Types of transportation problems, mathematical models, transportation algorithms



Assignment: Allocation and assignment problems and models, processing of job through machines.

UNIT-III

Network Techniques: Shortest path model, minimum spanning Tree Problem, Max-Flow problem and Min-cost problem.

Project Management: Phases of project management, guidelines for network construction, CPM and PERT.

UNIT-IV

Theory of Games: Rectangular games, Min-max theorem, graphical solution of $2 \times n$ normal form games, game with mixed strategies, reduction to linear programming model.

Quality Systems: Elements of Queuing model, generalized Poisson queuing model.

UNIT-V

Inventory Control: Models of inventory, operation of inventory system, quantity discount.

Replacement models: Equipments that deteriorate with time, equipments that fail with time.

TEXT/ REFERENCE BOOKS:

1. Wayne L. Winston, "Operations Research", Thomson Learning, 2003.
2. Hamdy H. Taha, "Operations Research - An Introduction", Pearson Education, 2003.
3. R. Panneer Seevam, "Operations Research", PHI Learning, 2008.
4. V. K. Khanna, "Total Quality Management", New Age International, 2008.

TEACHING METHODOLOGY

1. Lecture is delivered on blackboard, preparing OHP sheets and by preparing Power point presentations.
2. Seminars are conducted on new technologies related to subject.
3. Assignments are given.
4. Group discussions are conducted on familiar topics related to subject.
5. Industrial visits for practical exposure to understand and explore things.



II- SEMESTER





GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

CAD FOR VLSI CIRCUITS

M.Tech (VLSI)
Course Code: GR15D5099

I Year - II Semester
L/P/C: 4/0/4

COURSE OBJECTIVE

- To provide an introduction to the fundamentals of Computer-Aided Design tools for the modelling, design, analysis, test, and verification of digital Very Large Scale Integration (VLSI) systems.
- To study various physical design methods in VLSI
- To understand the concepts behind the VLSI design rules and routing techniques.
- To use the simulation techniques at various levels in VLSI design flow
- To understand the concepts of various algorithms used for floor planning and routing techniques.

COURSE OUTCOME: After going through the course students will be able to

- Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
- Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
- To practice the application of fundamentals of VLSI technologies
- Optimize the implemented design for area, timing and power by applying suitable constraints.
- To gain knowledge on the methodologies involved in design, verification and implementation of digital designs on reconfigurable hardware platform (FPGA)
- To gain knowledge on the methodologies involved in design, verification and implementation of digital designs on MCMs.
- To develop various algorithms at various levels of physical design.

UNIT-I

VLSI Physical Design Automation: VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles;

UNIT-II

Partitioning, Floor Planning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing, Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation,



Classification of pin assignment algorithms, General and channel Pin assignments, Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms;

UNIT-III

Global Routing and Detailed Routing: Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms;

UNIT-IV

Physical Design Automation of FPGAs: FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model;

Physical Design Automation of MCMs: Introduction to MCM Technologies, MCM Physical Design Cycle.

UNIT-V

Chip Input and Output Circuits: ESD Protection, Input Circuits, Output Circuits and noise, On-chip clock Generation and Distribution, Latch-up and its prevention.

TEXT BOOKS

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

CMOS MIXED SIGNAL CIRCUIT DESIGN

M.Tech (VLSI)
Course Code: GR15D5100

I Year - II Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- This course provides the concepts of switched capacitor circuits used in mixed signal circuit design.
- To know mixed signal circuits like DAC,ADC,PLL etc.,
- To acquire knowledge on design different architectures in mixed signal mode.
- To gain knowledge on noise shaping modulators and higher order modulators.
- It deals with the design and analysis of Biquad Filters.

COURSE OUTCOMES: After going through this course the student will be able to

- Analyze and design of switched capacitor circuits used in mixed signal circuit design
- Design noise shaping converters given a set of requirements such as bandwidth, clock speed and signal-to-noise ratio
- Design an integrated mixed signal circuit in CMOS using modern design tools
- Demonstrate in-depth knowledge in PLL and Data Converters (DAC and ADC)
- Analyze complex engineering problems critically for conducting research in data converters
- Solve engineering problems with wide range of solutions to increase data rate of ADC and DAC
- Apply appropriate techniques, resources to engineering activities in development of data converters.

UNIT -I

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT -II:

Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs- Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT -III:

Data Converter Fundamentals: DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters



UNIT -IV

Nyquist Rate A/D Converters: Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/Dconverters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT -V

Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Deltasigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press,International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche,Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
DESIGN FOR TESTABILITY

M.Tech (VLSI)
Course Code: GR15D5101

I Year - II Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To provide knowledge about VLSI Testing.
- To understand VLSI Technology Trends affecting Testing
- To get knowledge on Design verification and Test Evaluation
- Underlying the concept SCOAP Controllability and Observability
- To provide knowledge about testability Measures and methods
- To understand the concept of BIST architecture.
- To provide knowledge about Boundary Scan Test.

COURSE OUTCOMES

- Create understanding of the fundamental concepts of Testing in VLSI design.
- Perceiving Trends affecting Testing
- An ability to know Design verification and Test Evaluation.
- Employ the simulation algorithms for verification and validation
- An ability to know the high level testability measures and scan methods.
- An ability to know the BIST architecture: Test pattern generation, Circuit under test and Output response analyzer.
- Develop skills in modeling and evaluating Boundary Scan Standards.

UNIT -I:

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II:

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT -III:

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

**UNIT -IV:**

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V:

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BSDL Description Components, Pin Descriptions.

TEXT BOOKS

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Publishers.

REFERENCE BOOKS

1. Digital Systems and Testable Design - M. Abramovici, M.A. Breuer and A.D. Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

LOW POWER VLSI DESIGN

M.Tech (VLSI)
Course Code: GR15D5098

I Year - II Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To know about the need for low power circuit design.
- To provide strong foundation of fundamentals of low power circuit design.
- To furnish knowledge of various low power design approaches for VLSI System design.
- To analyze different low power design techniques.
- To develop different low voltage low power logic styles using low power techniques.
- To provide the design knowledge of various low power adders and multipliers.
- To develop the design knowledge of various low power memories.

COURSE OUTCOMES: After going through this course the student will be able to

- Student develops strong knowledge of fundamentals of low power VLSI circuit design.
- Student will be aware of various low power VLSI design approaches.
- Student will be aware of various low power logic styles.
- Student will be able to analyze all the low power design techniques.
- Student will develop the capability of designing low power data path subsystems such as adders and multipliers.
- Student will be equipped with technical knowledge to design low power memories for a VLSI system.
- Student will be able to design all low power circuit designs.

UNIT-I

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects – Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT-II

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach – Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.



UNIT-III

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques–Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT-IV

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT-V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – Anantha Chandrakasan, IEEE Press/Wiley International, 1998.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

DIGITAL SIGNAL PROCESSORS AND
ARCHITECTURES (Elective -III)

M.Tech (VLSI)
Course Code: GR15D5084

I Year - II Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To provide sound foundation of digital signal processing (DSP) architectures for designing efficient VLSI architectures for DSP systems.
- To analyze general purpose digital signal processors.
- To understand pipelining, parallel processing and retiming.
- To illustrate the features of on-chip peripheral devices and its interfacing along with its programming details.
- To analyze DSP architectures.

COURSE OUTCOMES: After going through this course the student will be able to An ability to design analog and digital filters for signal-processing applications.

- An ability to recognize the fundamentals of fixed and floating point architectures of various DSPs.
- An ability to learn the architecture details and instruction sets of fixed and floating point DSPs.
- An ability to Infer about the control instructions, interrupts, and pipeline operations.
- An ability to analyze and learn to implement the signal processing algorithms in DSPs.
- An ability to learn the DSP programming tools and use them for applications.
- An ability to design and implement signal processing modules in DSPs.

UNIT-I

Introduction to Digital Signal Processing: Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT-II

Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.



UNIT-III

Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT-IV

Analog Devices Family of DSP Devices: Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT-V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

VLSI SIGNAL PROCESSING
(Elective-III)

M.Tech (VLSI)
 Course Code: GR15D5103

I Year - II Semester
 L/P/C: 4/0/4

COURSE OBJECTIVES

- To expose the students to the concept of pipeline and parallel processing in VLSI
- To provide knowledge of realization of DSP system in VLSI.
- To train students to understand DSP algorithms Cook-Toom Algorithm, Fast Convolution algorithm by Inspection.
- To enable students to choose different parallel processing and pipeline processing techniques.
- To train students to know about minimization techniques.
- To enable students to Systolic Design for Space Representations contain Delays
- To train students towards Power Reduction techniques and Power Estimation techniques.

COURSE OUTCOMES: After going through this course the student will be able to

- Students will be able to design DSP system in VLSI.
- Students will be able to design low power systems.
- Students will be able to understand DSP algorithms Cook-Toom Algorithm, Fast Convolution algorithm by Inspection method.
- Students will be able to choose different parallel processing and pipeline processing techniques.
- Students will be able to understand minimization techniques.
- Students will be able to know Systolic Design for Space Representations contain Delays
- Students will be able to know Power Reduction techniques and Power Estimation techniques.

UNIT-I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power

Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT-II

Folding and Unfolding: Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems



Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT-III

Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT-IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT-V

Low Power Design: Scaling Vs Power Consumption – Power Analysis, Power Reduction techniques – Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. White House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.



GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

OPTIMIZATION TECHNIQUES IN VLSI DESIGN (Elective-IV)

M.Tech (VLSI)
Course Code: GR15D5104

I Year - II Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To understand the tradeoffs among various design styles given a set of design constraints in physical design automation and to understand performance/area tradeoffs in a chip design process.
- To learn the various statistic modeling methods like Monte Carlo techniques and Pelgromsmodel etc.,
- To learn the implementation issues for digital design automation including optimization techniques.
- To understand concept of design optimization algorithms and their application to physical design automation.
- To understand the latest design techniques as practiced in the Industry for design layout optimization.
- To expose students to the complexities and design methodologies of current and advanced VLSI design technologies.
- To understand the concepts of Physical Design Process such as Partitioning, Floor planning, Placement and Routing.

COURSE OUTCOMES: After going through this course the student will be able to

- Apply the appropriate design practices, emerging technologies, state-of-the-art design techniques, software tools, and research methods for IC design.
- Design the systems by using concepts of High level statistical, Gate level statistical analysis methods.
- Design the low power digital systems by applying appropriate partitioning and Floor planning algorithms.
- Design the real time applications using optimization techniques like Genetic Algorithms.
- Understand the concepts of geometric programming and convex functions.
- Apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
- Map the technology with latest FPGA

UNIT-I

Statistical Modeling: Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgromsmodel, Principle component based modeling, Quad tree based modeling,



Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

UNIT-II

Statistical Performance, Power and Yield Analysis: Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, Highlevel statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT-III

Convex Optimization: Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

UNIT-IV

Genetic Algorithm: Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybridgenetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement-GASPalgorithm-unified algorithm.

UNIT-V

GA Routing Procedures and Power Estimation: Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-testgeneration procedures, Power estimation-application of GA-Standard cell placement-GA for ATGproblemencoding- fitness function-GA Vs Conventional algorithm.

TEXT BOOKS / REFERENCE BOOKS

1. Statistical Analysis and Optimization for VLSI: Timing and Power - Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation - Pinaki Mazumder, E. Mrudnick, Prentice Hall, 1998.
3. Convex Optimization - Stephen Boyd, Lieven Vandenberghe, Cambridge University Press, 2004.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

SYSTEM ON CHIP ARCHITECTURE
(Elective -IV)

M.Tech (VLSI)
Course Code: GR15D5091

I Year - II Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To describe the system design approach with respect to the hardware and software
- To apply the techniques for reducing the delays in program execution
- To categorize and compare different processor types for their selection into a System on Chip.
- To compare different memory designs and their purposes
- To interpret the architectures and applications of various buses.
- To analyze and choose from different reconfigurable devices for a system on chip.
- To interpret the standard algorithms like AES.

COURSE OUTCOMES: After going through this course the student will be able to

- Students will be able to summarize all the components required for system design.
- Students will be acquired the techniques to minimize the delays for better performance of a system on chip.
- Students will be acquired with the analytical skill to decide what type of processor is required to design anSoC for the undersigned application.
- Students will be calibre to classify the types and applications of different memory devices.
- Students will be able to analyze different types of buses for respective applications.
- Students will be skilful to judge a configurable device based on the application requirement for a system on chip
- Students will have the technique to implement AES algorithm if required.

UNIT-I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT-II

Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.



UNIT-III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT-IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance-Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT-V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiley India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

**SEMICONDUCTOR MEMORY DESIGN AND
 TESTING (Elective-IV)**

M.Tech (VLSI)
 Course Code: GR15D5105

I Year - II Semester
 L/P/C: 4/0/4

COURSE OBJECTIVES

- To train students to design different architectures for various SRAM and DRAM technologies.
- To enable students to choose different non-volatile memories conditionally.
- To enable students to model the faults and design memories for testability and fault tolerance.
- To enable students to design reliable memories and to overcome effects of radiation.
- To enable students to use advanced memory technologies, various high density memories and packages.

COURSE OUTCOMES: The graduate student can design various memory architectures.

- Will be able to analyze and choose non-volatile memories based on the application.
- Will be able to model the faults.
- Will be able to design fault tolerant memory systems.
- Will be able to design reliable memory architectures by considering radiation effects.
- Can choose and design various high density memories for different applications.
- Can choose packages for memories.

UNIT-I

Random Access Memory Technologies: SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM

UNIT-II

Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT-III

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM



fault modeling, BIST techniques for memory

UNIT-IV

Semiconductor Memory Reliability and Radiation Effects: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Wafer Level Radiation Testing and Test structures

UNIT-V

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magnetoresistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

TEXT BOOKS

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., PrenticeHall.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

VLSI LAB-II

M.Tech (VLSI)
Course Code: GR15D5106

I Year - II Semester
L/P/C: 4/0/4

COURSE OBJECTIVES

- To provide the practical design knowledge of VLSI circuits using CAD tools.
- To provide practical knowledge of Gate level design and Transistor level design.
- To draw the schematic and layouts of design using Cadence Virtuoso tool
- To describe practical knowledge of Simulation and Verification for integrated circuits.
- To provide design capability of circuit at layout level and verification after extraction of parasitics.
- To provide knowledge of implementing various VLSI circuits.

COURSE OUTCOMES: After going through this course the student will be able to

- Analyze practical implementation of digital and analog circuits
- Develops an ability to know the CAD tools to design VLSI circuits.
- Develops an ability to draw the Layout of any combinational circuits.
- Gain knowledge in Verification of the Circuit.
- Perform timing and power analysis using Cadence tools
- Develop skills in SPICE simulation and Analog Circuit simulation
- Develops an ability to build the VLSI System level design.

Note: All the following digital/analog circuits are to be designed and implemented using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.

The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL orVHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and backannotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

VLSI Back End Design programs:

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR dropanalysis and crosstalk analysis of the following:
 - CMOS inverter
 - CMOS NOR/ NAND gates
 - CMOS XOR and MUX gates



- CMOS half adder and full adder
 - Static / Dynamic logic circuits (register cell)LatchPass transistor
3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths
 4. Introduction to SPICE simulation and coding of NMOS/CMOS circuit
 5. SPICE simulation of basic analog circuits: Inverter / Differential amplifier
 6. Analog Circuit simulation (AC analysis) – CS & CD amplifier
 7. System level design using PLL



OPEN ELECTIVE - II





GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

HUMAN COMPUTER INTERACTION
(Open Elective-II)

M.Tech (CSE)
Course Code: GR15D5184

I Year - II Semester
L/P/C: 4/0/4

COURSE OBJECTIVES: Students undergoing the course are expected to:

- Demonstrate an understanding of guidelines, principles, and theories influencing human computer interaction.
- Recognize how a computer system may be modified to include human diversity.
- Select an effective style for a specific application.
- Design mock ups and carry out user and expert evaluation of interfaces.
- Carry out the steps of experimental design, usability and experimental testing, and
- Evaluation of human computer interaction systems.
- Use the information sources available, and be aware of the methodologies and technologies supporting advances in HCI.

COURSE OUTCOMES: At the end of the course, the student will be able to:

- Describe what interaction design is and how it relates to human computer interaction and other fields.
- Describe the social mechanisms that are used by people to communicate and collaborate.
- Describe how technologies can be designed to change people's attitudes and behavior.
- Discuss how to plan and run a successful data gathering program.
- Discuss the difference between qualitative and quantitative data and analysis.
- Discuss the conceptual, practical, and ethical issues involved in evaluation.
- Describe how to perform two types of predictive techniques, GOMS and Fitts Law, and when to use them.

UNIT-I

Introduction: Importance of user Interface –definition, importance of good design. Benefits of good design. A brief history of Screen design. The graphical user interface –popularity of graphics, the concept of direct manipulation, graphical system, Characteristics, Web user – Interface popularity, characteristics-Principles of user interface.

UNIT-II

Design process: Human interaction with computers, importance of human characteristics human consideration, Human interaction speeds, Understanding business junctions.

UNIT-III

Screen Designing: Design goals –Screen planning and purpose, organizing screen elements, ordering of screen data and content –screen navigation and flow –Visually pleasing composition



–amount of information –focus and emphasis –presentation information simply and meaningfully
–information retrieval on web –statistical graphics –Technological consideration in interface design.

UNIT-IV

Develop System Menus and Navigation Schemes-Select the proper kinds of Windows, -Select the proper Device based Controls, Choose the proper screen based controls.

UNIT-V

Mobile Ecosystem: Platforms, Application frameworks- Types of Mobile Applications: Widgets, Applications, Games- Mobile Information Architecture, Mobile 2.0, Mobile Design: Elements of Mobile Design, Tools.

Interaction Devices – Keyboard and Function Keys – Pointing Devices – Speech Recognition Digitization and Generation – Image and Video Display – Drivers.

TEXT BOOKS

1. The essential guide to user interface design, Wilbert O Galitz, Wiley Dreamtech.
2. Designing the user interface. 3rd Edition Ben Shneidermann, Pearson Education Asia
3. Brian Fling, "Mobile Design and Development", First Edition, Reilly Media Inc., 2009

REFERENCE BOOKS

1. Human – Computer Interaction. Alan Dix, Janet Fincay, GreGoryd, Abowd, Russell Bealg, Pearson Education
2. Interaction Design Prece, Rogers, Sharps. Wiley Dreamtech.
3. User Interface Design, Soren Lauesen, Pearson Education.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

BIG DATA ANALYTICS
(Open Elective-II)

M.Tech (IT)

Course Code: GR15D5185

I Year - II Semester

L/P/C: 4/0/4

COURSE OBJECTIVES: The objective of the course is to provide the student:

- Understanding about big data for business intelligence
- Learning business case studies for big data analytics
- Learning about the cloud and big data
- Knowledge about risk management involved in big data
- Understanding nosql big data management
- Understanding about map reduce work flows.
- Capability to Perform map-reduce analytics using Hadoop and related tools

COURSE OUTCOMES: At the end of the course the student will be able to:

- Understand the importance of big data
- Understand challenges with big data
- Knowledge about the technological developments in big data environment
- Understanding about map reduce work flows
- Knowledge about nosql data environment.
- Analysis with Hadoop and related tools
- Capability of understanding the usage of big data in context to cloud and other technologies.

UNIT-I

INTRODUCTION TO BIG DATA What is big data, why big data, convergence of key trends , unstructured data ,industry examples of big data ,web analytics, big data and marketing, fraud and big data ,risk and big data ,credit risk management, big data in medicine, introduction to Hadoop open source technologies , cloud and big data

UNIT-II

UNDERSTANDING BIG DATA Types of digital data, characteristics of data, challenges with big data, definition of big data, big data analytics, data science, technologies in big data environments, CAP theorem.

UNIT-III

NOSQL DATA MANAGEMENT Introduction to NoSQL, aggregate data models, aggregates, key-value and document data Models, relationships, graph databases , schemaless databases ,materialized views, distribution models, sharding ,master-slave replication, peer-peer replication, sharing and replication



UNIT-IV

BASICS OF HADOOP Data format ,features of Hadoop, analyzing data with Hadoop , design of Hadoop distributed file system (HDFS) ,HDFS concepts, scaling out ,Hadoop streaming , Hadoop pipes, Hadoop related tools

UNIT- V

MAPREDUCE APPLICATIONS MapReduce workflows, unit tests with MRUnit , test data and local tests, anatomy of MapReduce job run ,classic Map-reduce, YARN ,failures in classic Map-reduce and YARN , job scheduling , shuffle and sort ,task execution, MapReduce types ,input formats, output formats

TEXT BOOKS

1. Seema Acharya,S.Chellappan,"Big Data and Analytics",Wiley,2014

REFERENCE BOOK

1. Michael Minelli, Michelle Chambers, and AmbigaDhiraj, "Big Data, Big Analytics: Emerging Business Intelligence and Analytic Trends for Today's Businesses", Wiley, 2013.
2. P. J. Sadalage and M. Fowler, "NoSQL Distilled: A Brief Guide to the Emerging World of Polyglot Persistence", Addison-Wesley Professional, 2012.
3. Tom White, "Hadoop: The Definitive Guide", Third Edition, O'Reilley, 2012.
4. Eric Sammer, "Hadoop Operations", O'Reilley, 2012.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

NEURAL AND FUZZY SYSTEMS
(Open Elective-II)

M.Tech (EEE)
Course Code: GR15D5186

I Year - II Semester
L/P/C: 4/0/4

PRE–REQUISITE: Control Systems, Power Systems, Mathematics, Physics.

COURSE OBJECTIVES: The objective of the course is to provide the student

- To introduce the students with the concepts of learning methods.
- To provide students with the artificial neural networks and their architecture.
- To familiarize the students with the various applications of artificial neural networks.
- To introduce the concepts of the fuzzy logic control and their real time applications.

COURSE OUTCOMES: At the end of the course the student will be able to

- Define the advances in neural networks
- Evaluate the design and control of fuzzy systems.
- Articulate the applications of fuzzy control block sets.
- Evaluate the design of various models in neural networks
- To analyze the techniques of various types of neural networks
- Evaluate the design and control of associative memories
- Techniques to Design fuzzy logic system

UNIT-I

Introduction to Neural Networks: Introduction, Humans and Computers, Organization of the Brain, Biological Neuron, Biological and Artificial Neuron Models, Hodgkin-Huxley Neuron Model, Integrate-and- Fire Neuron Model, Spiking Neuron Model, Characteristics of ANN, McCulloch-Pitts Model, Historical Developments, Potential Applications of ANN.

UNIT-II

Essentials of Artificial Neural Networks: Artificial Neuron Model, Operations of Artificial Neuron, Types of Neuron Activation Function, ANN Architectures, Classification Taxonomy of ANN – Connectivity, Neural Dynamics (Activation and Synaptic), Learning Strategy (Supervised, Unsupervised, Reinforcement), Learning Rules, Types of Application

Feed Forward Neural Networks

Introduction, Perceptron Models: Discrete, Continuous and Multi-Category, Training Algorithms: Discrete and Continuous Perceptron Networks, Perceptron Convergence theorem, Limitations of the Perceptron Model, Applications.



UNIT-III

Multilayer Feed forward Neural Networks

Credit Assignment Problem, Generalized Delta Rule, Derivation of Backpropagation (BP) Training, Summary of Backpropagation Algorithm, Kolmogorov Theorem, Learning Difficulties and Improvements.

Associative Memories

Paradigms of Associative Memory, Pattern Mathematics, Hebbian Learning, General Concepts of Associative Memory (Associative Matrix, Association Rules, Hamming Distance, The Linear Associator, Matrix Memories, Content Addressable Memory), Bidirectional Associative Memory (BAM) Architecture, BAM Training Algorithms: Storage and Recall Algorithm, BAM Energy Function, Proof of BAM Stability Theorem Architecture of Hopfield Network: Discrete and Continuous versions, Storage and Recall Algorithm, Stability Analysis, Capacity of the Hopfield Network.

UNIT-IV

Self-Organizing Maps (SOM) and Adaptive Resonance Theory (ART)

Introduction, Competitive Learning, Vector Quantization, Self-Organized Learning Networks, Kohonen Networks, Training Algorithms, Linear Vector Quantization, Stability-Plasticity Dilemma, Feed forward competition, Feedback Competition.

UNIT-V

Classical and Fuzzy Sets and Fuzzy Logic System Components

Introduction to classical sets - properties, Operations and relations; Fuzzy sets, Membership, Uncertainty, Operations, properties, fuzzy relations, cardinalities, membership functions.

Fuzzification, Membership value assignment, development of rule base and decision making system, Defuzzification to crisp sets, Defuzzification methods.

Applications Neural network applications: Process identification, Function Approximation, control and Process Monitoring, fault diagnosis and load forecasting.

Fuzzy logic applications: Fuzzy logic control and Fuzzy classification.

TEACHING METHODOLOGIES

1. White board
2. PPTs
3. Seminars

TEXT BOOK

1. Neural Networks, Fuzzy logic, Genetic algorithms: synthesis and applications by Rajasekharan and G.A.VijayalakshmiPai – PHI Publication.

REFERENCE BOOKS

1. Introduction to Artificial Neural Systems - Jacek M. Zurada, Jaico Publishing House, 1997.
2. Neural Engineering by C.Eliasmith and CH.Anderson, PHI
3. Neural Networks and Fuzzy Logic System by Bork Kosko, PHI Publications



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

PROJECT MANAGEMENT
(Open Elective-II)

M.Tech(Civil)

Course Code: GR15D5187

I Year - II Semester

L/P/C: 4/0/4

COURSE OBJECTIVES: On completion of this Subject/Course, following objectives shall get accomplished

- To provide students about the basics of Management in general and Project Management in particular.
- To train the students about the Monitoring of Projects.
- To make understand the students about the Planning of projects.
- To make understand the students about the Scheduling of projects.
- To train the students about the drawing of CPM & PERT Networks.
- To train the students about teaching of Project Management to UG & PG students
- To motivate the students about the Research Development activities of Project Management which results in timely completion of projects without time and cost over runs.

Course outcomes: On completion of this Subject/Course the student shall be able to

- Perform the Project Management functions effectively.
- Plan the projects.
- Schedule the various activities of Projects.
- Monitor the actual progress with planned progress.
- Draw the CPM & PERT Networks/
- Handle Resources planning including levelling & smoothing.
- Interpret the Indian Contract Act and understand the litigations involved for better Contract Management.

UNIT- I

PROJECT PLANNING: Prime Objectives of Project Management, Main Functions of Project Management, Planning, Principles of Planning, Objectives of Planning, Steps involved in Planning, Stages of Planning, Advantages & limitations of Planning, Failures of Projects & Construction Projects.

UNIT-II

PROJECT SCHEDULING: Scheduling, Project/Construction Schedules, Steps involved in Scheduling, Methods of Scheduling, Bar Charts, Steps involved in Bar Charts, Limitations of Bar Charts, Milestone Charts and Limitations of Milestone Charts.



UNIT-III

PROJECT MONITORING: Network Techniques, Prime Objectives of Networks, Network Terminology, Types of Networks, CPM & PERT, Differences between CPM & PERT, Rules to draw the Network, Drawing of Networks, Advantages of Network , Critical Path, Float and its Types, Slack and Types of Slack.

UNIT-IV

PROJECT COST CONTROL: Direct Costs, Indirect Costs, Total Project Cost, Optimisation of Cost and Steps involved, Resources, Resources Smoothing and Resources Levelling, Crashing of Activities, Time and Cost Over runs of Project.

UNIT-V

PROJECT QUALITY & CONTRACTS:

Quality, Quality Control, Quality Assurance, Project Quality Plans in Construction Projects, Inspection & Test Plans, Method Statements, ISO Certification; Project Contracts, Contract Law, Types of Contracts and Indian Contract Act.

TEXT BOOKS

1. Project Planning and Control with PERT & CPM – BC Punmia, KK Khandielwala.
2. Project Scheduling & Monitoring in Practice – S Chowdhury

REFERENCE BOOKS

1. Project Management Handbook – Lock, Gower
2. Project Management – NJ Smith- Blackwell Publication.



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

HARDWARE - SOFTWARE CO-DESIGN
(Open Elective-II)

M.Tech (ECE)
Course Code: GR15D5188

I Year - II Semester
L/P/C: 4/0/4

Course Objectives

- Describe an embedded system design flow from specification to physical realization
- Describe structural behavior of systems.
- Master complex systems.
- Devise new theories, techniques, and tools in design, implementation and testing.
- Master contemporary development techniques.

Course Outcomes: After going through this course the student will be able to

- Gain knowledge of contemporary issues and algorithms used.
- Know the interfacing components, different verification techniques and tools.
- Demonstrate practical skills in the construction of prototypes.
- Understand the use of modern hardware and software tools for building prototypes of embedded systems.
- Apply embedded software techniques to satisfy functional and response time requirements.
- Apply verification tools.
- Understand design representation for system level synthesis.

UNIT-I:

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms:

Hardware software synthesis algorithms: hardware – software partitioning distributed system cosynthesis.

UNIT –II:

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.



UNIT-III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT-IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT-V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 –Springer



GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
NON CONVENTIONAL ENERGY RESOURCES
(Open Elective-II)

M.Tech (ME)
 Course Code: GR15D5189

I Year - II Semester

Course Objectives: The Objective of this course is to provide the student to

- Interduce the need of the non-convectional energy sources.
- Impart the role of non-convectional energy for the environment.
- Identify the energy resources utilization systems.
- Recognise the source and potential of wind energy and understand the classifications of wind mills.
- Summarize the principles of bio-conversion, ocean energy and geo thermal energy.

Course Outcomes: At the end of the course the learners will be able to

- Choose the appropriate renewable energy as an alternate for conventional power in any application.
- Analyze the environmental and cost economics of using renewable energy sources compared to fossil fuels.
- Apply the principles of various energy systems in day to day life.
- Analyze the industrial needs and convert theoretical model to practical circuits with wide range of specifications.
- Evaluate the importance of the renewable resources of energy as the fossil fuels are depleting in the world very fast express about clean and green energy for next generation.
- Analyse large scale demand of heat energy for meeting day to day domestic, institutional and industrial requirements can be met by utilizing solar thermal systems, biogas, PV cells, wind energy, Geothermal, MHD etc.
- Design the various techniques and models fabricated in utilizing the above said sources of energy.

UNIT-I

Introduction: Various non-conventional energy resources-Introduction, availability, classification, relative merits and demerits.

Solar Cells: Theory of solar cells. solar cell materials, solar cell array, solar cell power plant, limitations.

UNIT-II

Solar Thermal Energy: Solar radiation, flatplate collectors and their materials, applications and performance, focusing of collectors and their materials, applications and performance; solar thermal power plants, thermal energy storage for solar heating and cooling, limitations.



UNIT-III

Geothermal Energy: Resources of geothermal energy, thermodynamics of geo-thermal energy conversion-electricalconversion, non-electricalconversion,environmentalconsiderations.

Magneto-hydrodynamics (MHD):

Principle of working of MHD Power plant, performance and limitations

FuelCells:

Principle of working of various type souffle cell sand their working, performance and limitations.

UNIT-IV

Thermos and the rmionic Conversions:

Principle of working, performance and limitations.

Wind Energy: Wind power and it surcease, sites election, criterion, momentum theory, classification of rotors, concentrations and augments, wind characteristics. Performance and limitation sofenergy conversion systems.

UNIT-V

Bio-mass:Availability of bio-massand its conversion theory.

Ocean Thermal Energy Conversion (OTEC):

Availability, theory and working principle, per formance and limitations.

Wave and Tida IWave:

Principle of working, performance and limitations.Waste RecyclingPlants.

TEXT/REFERENCESBOOKS

1. John Twideu and TonyWeir, "Renewal Energy Resources" BSP Publications, 2006.
2. M.V.R.KoteswaraRao, "Energy Resources: Conventional&Non-Conventional " BSPPublications,2006.
3. D.S.Chauhan, "Non-conventional Energy Resources" New Age International.
4. C.S. Solanki, "Renewal Energy Technologies: A Practical Guidefor Beginners" PHILearning.